

Data
Systems

PHILIPS

Field Support Manual
P4000 - 24 (WMD)
MOS Memory Module 128K16

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1 GENERAL DESCRIPTION

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1.1 INTRODUCTION

This manual describes a volatile Main Memory Module for UPL-systems.
Technically there are three versions: 128K16, 64K16 and the 32K16 version.
Standard capacity will be 128K16 (full memory module with 64K devices); also half populated versions of 64K16 are possible.
In case of 16K (+5V only) devices are applied, only full memory modules of 32K16 are possible.
The PCB contains the complete timing and control for the memory devices and the UPL-interface.
It's possible to write or read in either word- or character mode.
The memory module contains error correction for one failing bit of a word of 16 bits.
By means of the card select logic on the cards it is possible to have more cards in parallel.
Depending on the computer system it is possible to intermix this module with other MOS memory types.
The maximum configuration of the memory is in any case 16M.
The name of the PCB is WMD.

1.2 PHYSICAL DESCRIPTION

The memory has been designed on a single board of the "Double Euro Card" format.
The card is connected to the system bus with one connector on the backpanel.

DIMENSIONS

- width : 233,4mm
- length : 160mm
- component height : less than 8,5mm
- solder length : less than 2,5mm
- mounting distance : less than or equal to 0,6 inch

1.3 TECHNICAL DATA

1.3.1 PERFORMANCE DATA

Cycle	ACN access time			TSMN access time			MEN[4]	Bus cycle [5]		
	min[3]	typ	max[3]	min[3]	typ	max[3]	CYCLE	min	typ	max
READ no error detected	130	195	267	507	570	642	625	564	683	748
READ error corrected	130	195	267	632	694	767	687.5	626	745	810
WRITE word	130	195	267	130	195	267	625	502	585	670
WRITE character	130	195	267	130	195	267	1250	1127	1210	1295

Table 1.1 ACCESS AND CYCLE TIMES

1. Timing figures without the influence of refresh.
2. Access time figures are given accordance UPL specifications for new memories.
3. The min. and max. access time figures include a worst case (max) or best case (min) synchronisation time.
   In case that the master synchronizes the TMRN with its own clock (no straight TTL or RC delay between TSMN rising edge and the falling edge or TMRN), one may calculate with a long term average min. or max. time.
   For min. average add 32 ns to min. time.
4. Internal memory cycle time.
5. Assuming t_1 + TSMN $\downarrow$ to TMRN $\uparrow$ = 0 ns

   t_2 : TSMN $\uparrow$ to TMRN $\downarrow$ = 50 ns

1.3.2 POWER REQUIREMENTS

The power supply for the memory module comes via the connector on the system bus and consists of +5VL, +5VM. The exact voltages and conditions are given in figure 1.1.

	Voltage V	max. average current			d I max.	f max.	C0	C1	L1	C2	L2	max. rate-ing
		opera-ting	stand-by	stand-by batt.								
+5VL	5.05V±4%	1.3A	1.3A	0A	0.2A	0.5Mc	1nF	1uF	-	33uF	20nH	+7V
+5VM	5.05V±1%	1.25A')	0.9A	0.9A	1.6A	2Mc	2nF	2.5uF	-	133uF	5nH	+7V

') Based on memory request rate of 1 usec.

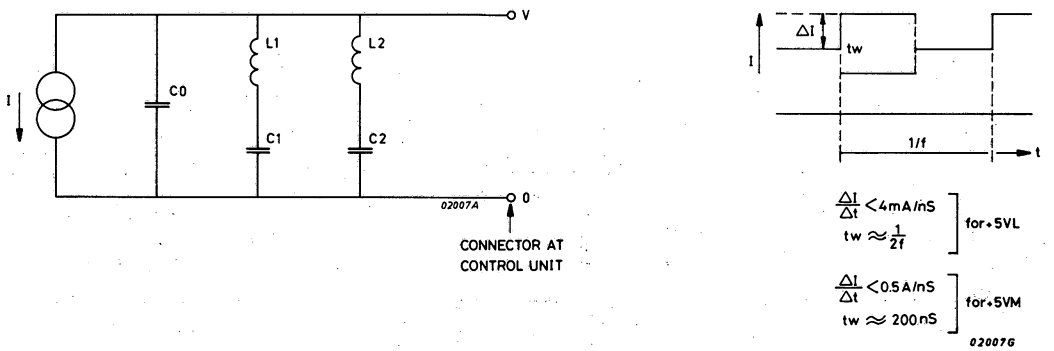


Figure 1.1 POWER REQUIREMENTS FOR THE MEMORY MODULE

1.3.3 PHYSICAL CHARACTERISTICS

A drawing which gives all dimensions of the card is given in figure 1.2. Also the location of the device plugs and the coordinates are included in this figure.

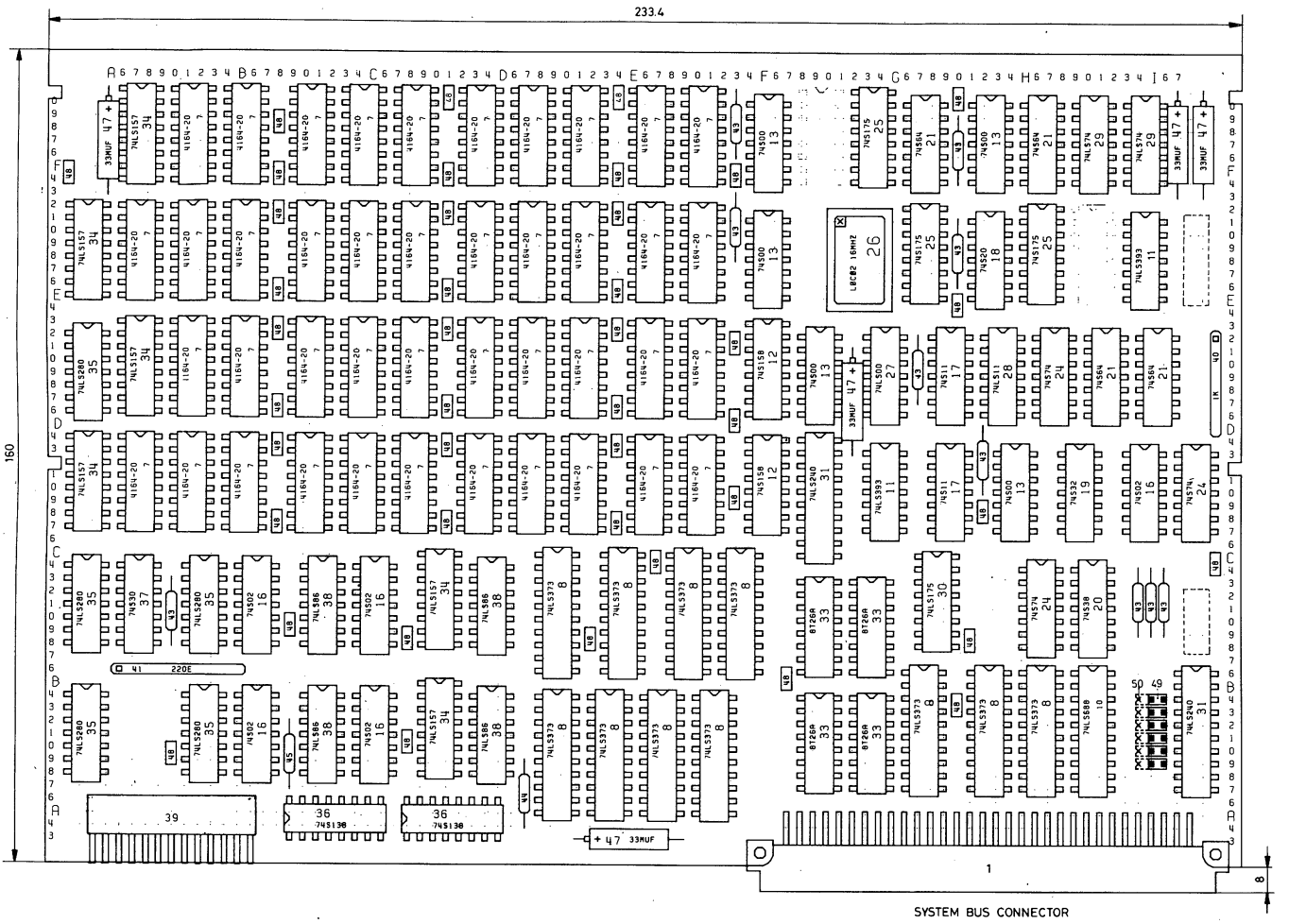


Figure 1.2 CARD LAYOUT

The connector to the system interface is 96-pins male connector. In figure 1.3 the dimensions and pin numbering are indicated.

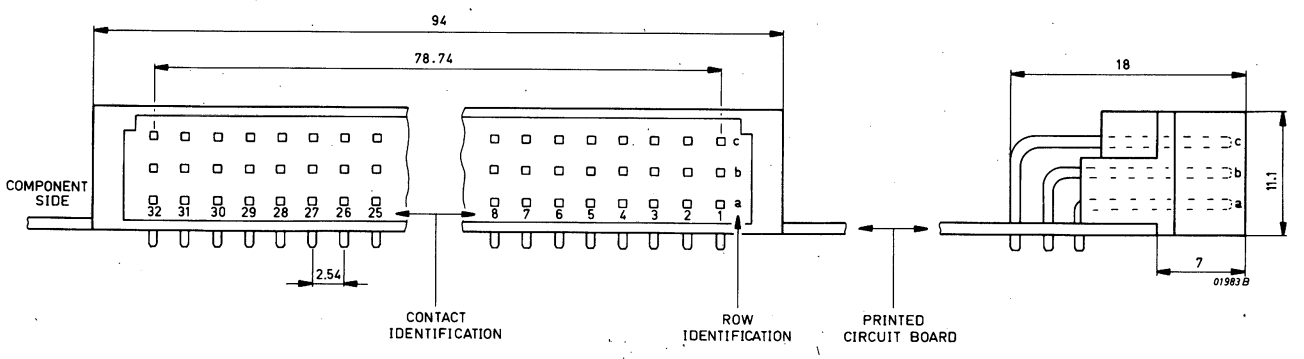


Figure 1.3 BOTTOM VIEW AND SIDE VIEW OF THE SYSTEM INTERFACE CONNECTOR

1.3.4 ENVIRONMENTAL CONDITIONS

	TEMPERATURE		REL. HUMIDITY	
	MIN.	MAX.	MIN.	MAX.
ABSOLUTE OPERATING LIMITS	5°C	40°C	10%	98%
OPTIMUM OPERATING LIMITS	12°C	32°C	20%	90%

The dynamic limits dT = 10°C / ½ hour.
The air velocity between the cards must be more than 1.5m/sec.

Table 1.2 OPERATING CONDITIONS

TEMPERATURE		REL. HUMIDITY	
MIN.	MAX.	MIN.	MAX.
+3°C	+50°C	10%	90%

The dynamic limit dT = 10°C / 1 hour.

	PACKED		UNPACKED	
	MIN.	MAX.	MIN.	MAX.
TEMPERATURE	-40°C	+70°C	-40°C	+70°C
REL. HUM. 12 HOURS	10%	100%	10%	90%
REL. HUM. 6 WEEKS	10%	98%	10%	90%
REL. HUM. 3 MONTHS	10%	90%	10%	90%

The dynamic limit dT = 30°C / 5 minutes.

Table 1.3 STORAGE CONDITIONS

	MIN.	MAX.
OPERATING LIMITS	700 mbar	1100 mbar
NON-OPERATING LIMITS	450 mbar	1100 mbar

700 mbar is an altitude of approximately 2250 meters above sea-level.
450 mbar is an altitude of approximately 6300 meters above sea-level.

Table 1.4 AIR PRESSURE

1.4 INTERFACES

1.4.1 THE SYSTEM BUS CONNECTOR

NAME	DESCRIPTION
ACN	"Acknowledge" indicates the release time for bus-signals.
BIØOO-15N	16 Data-lines of the System Bus.
CHA	"Character" is set by the Master indicating that a character or a word is transferred via the bus.
MADOO-15	The last significant two octads of the bus address lines.
MADEO-7	The most significant octad of the bus address lines.
RSLN	"Reset line"
TMRN	"Timing Master to RAM not"
TSMN	"Timing Slave to Master not"
WRITE	Indicating during data transfer if the data has to be read or written from/to memory.

Table 1.5 INTERFACE SIGNALS

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01	+12VL *	1B01	ERQN *	1A01	-12VL *
1C02	+ 5VM	1B02	BUSRN *	1A02	+ 5VM
1C03	BCI *	1B03	MSN *	1A03	INCL *
1C04	- *	1B04	OV	1A04	- *
1C05	- *	1B05	BSYN *	1A05	- *
1C06	OV	1B06	OKO *	1A06	OV
1C07	PWFN *	1B07	OKI *	1A07	RSLON
1C08	CLEARN *	1B08	RTCN *	1A08	ACN
1C09	OV	1B09	BAWOFN *	1A09	OV
1C10	TMPN *	1B10	STOPN *	1A10	TSMN
1C11	TMEN *	1B11	OV	1A11	TMRN
1C12	OV	1B12	MADE0	1A12	OV
1C13	MAD00	1B13	MADE1	1A13	MAD01
1C14	MAD02	1B14	OV	1A14	MAD03
1C15	MAD04	1B15	MADE2	1A15	MAD05
1C16	MAD06	1B16	MADE3	1A16	MAD07
1C17	MAD08	1B17	MADE4	1A17	MAD09
1C18	MAD10	1B18	MADE5	1A18	MAD11
1C19	MAD12	1B19	MADE6	1A19	MAD13
1C20	MAD14	1B20	MADE7	1A20	MAD15
1C21	CHA	1B21	OV	1A21	WRITE
1C22	OV	1B22	- *	1A22	OV
1C23	BI008N	1B23	- *	1A23	BI000N
1C24	BI009N	1B24	- *	1A24	BI001N
1C25	BI010N	1B25	- *	1A25	BI002N
1C26	BI011N	1B26	OV	1A26	BI003N
1C27	BI012N	1B27	- *	1A27	BI004N
1C28	BI013N	1B28	- *	1A28	BI005N
1C29	BI014N	1B29	- *	1A29	BI006N
1C30	BI015N	1B30	- *	1A30	BI007N
1C31	+12VM *	1B31	+5VL	1A31	+12VM *
1C32	+5VL	1B32	+5VL	1A32	+5VL

* not used

Figure 1.4 CONNECTOR LAYOUT

1.4.2 TEST CONNECTER

SIGNAL DESCRIPTION

Name	Description
EC DSO-4	Output, memory syndrome (E.C.) bits
TERRORN	Input, a low indicates the detection of an error
TSBITO-4	Input, data for the memory syndrome bits
TBLEC D	Input, a "1" blocks the normal memory data to the ECC
TBLECDS	Input, a "1" blocks the memory syndrome data to the ECC
TBLRFN	Input, a "0" blocks the refresh actions
SF	Output, indicates a single fail

Table 1.6 TEST CONNECTOR SIGNALS

ELECTRICAL CHARACTERISTICS

Outputs EC DSO-4 I less than or equal to -2 mA
at V =0,5V ,C greater than or equal to 10pF

TERRORN) I greater than or equal to 0,1 mA
) at V =2,4V

Inputs	I_{IL} at V_{IL} = 0.5V	I_{IH} at V_{IH} = 2.4V
TSBITO-4	3 mA	12 mA
TBLECDS	12 mA	48 mA
TBLECD	16 mA	80 mA
TBLRFN	- 6 mA	- 3 mA
TBLECN	-11 mA	- 3 mA

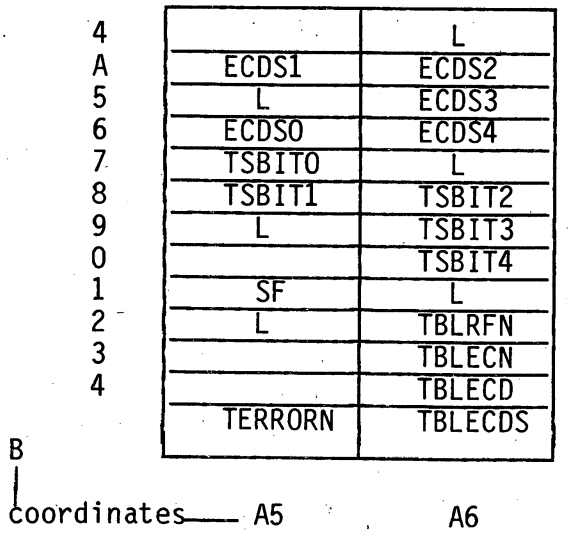


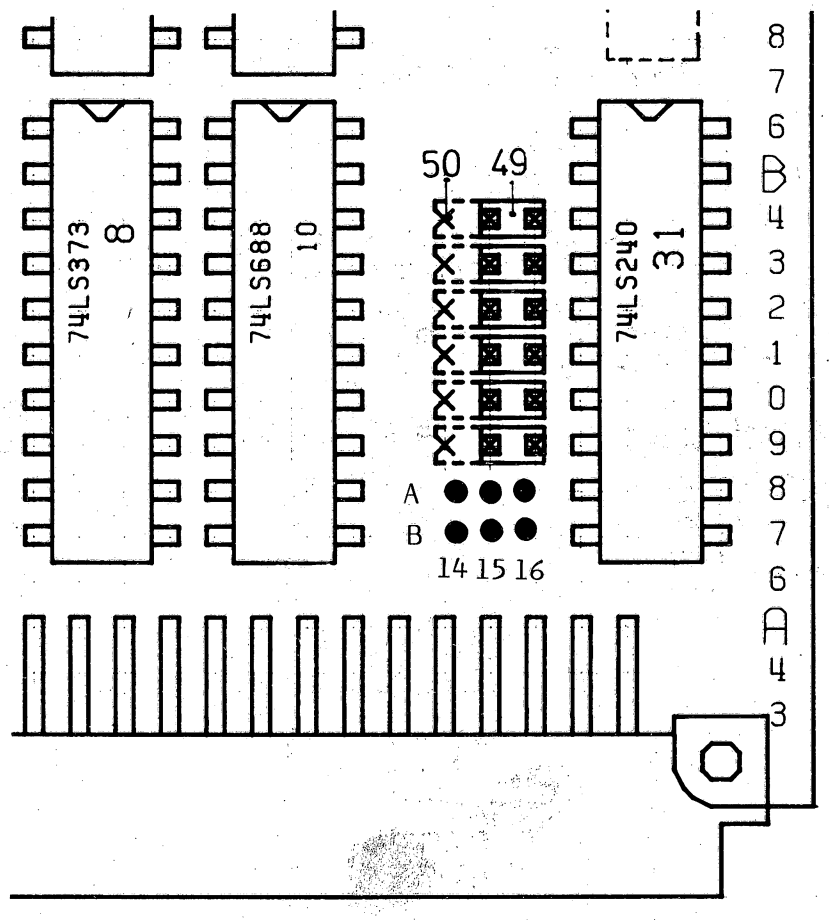
Figure 1.5 TEST CONNECTOR LAYOUT

1.5 APPLICATION NOTES

This memory module can be used in any system with the restriction that the system must be equipped with UPL interface. It's possible to intermix the WMD with other UPL memories, with the restriction that the start-address is a multiple of 128K16 for 128K16 module.

1.6 INSTALLATION DATA

1.6.1 STRAPSETTINGS



Depending of the module capacity also straps at the location indicated with a) and b) can be placed.

	I4	I5	I6	
B4	o	o	o	MADE0
B3	o	o	o	MADE1
B2	o	o	o	MADE2
B1	o	o	o	MADE3
B0	o	o	o	MADE4
A9	o	o	o	MADE5
A8	o	o	o	MADE6*
A7	o	o	o	MADE7**
	H		L	

	MADE	0	1	2	3	4	5	MODULE No
0 - 128K16		L	L	L	L	L	L	0
128 - 256K16		L	L	L	L	L	H	1
256 - 384K16		L	L	L	L	H	L	2
384 - 512K16		L	L	L	L	H	H	3
- 8M16		H	H	H	H	H	H	63

* not placed for the 128K16 module
** not placed for the 128K16 and 64K16 module

Figure 1.6 STRAPSETTING

For the 64K16 and the 32K16 modules is the strapsetting the same, except that the start-address is 64K16 x MODULE No for 64K16 module and 32K16 x MODULE No for the 32K16 module.

1.6.2 MOUNTING

The physical location of the memories are depending on the system where they have to be mounted. Only two modules are to be mounted in a system.

1.6.3 INTERCONNECTIONS

Only one interface exists. See section 1.4.

1.6.4 COMPATIBILTY

Not applicable.

2 FUNCTIONAL DESCRIPTION

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	2.8	READ RIGHT CHARACTER	2-10

2 FUNCTIONAL DESCRIPTION

The memory card can be distinguished in the following main blocks:

1. Memory Matrix/Memory Device
2. Addressing
3. Data I/O
4. Refresh
5. Control and Timing
6. Error Correction

2.1 MEMORY MATRIX/MEMORY DEVICE

MEMORY MATRIX

The complete memory array is build up of two bars by 21 columns (5 for error correction) of 64K1 random access dynamic MOS read, write memory devices.

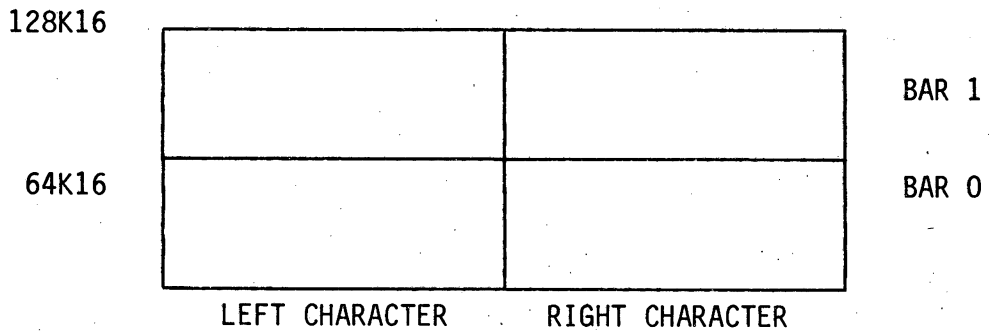


Figure 2.1 MEMORY MATRIX

MEMORY DEVICE

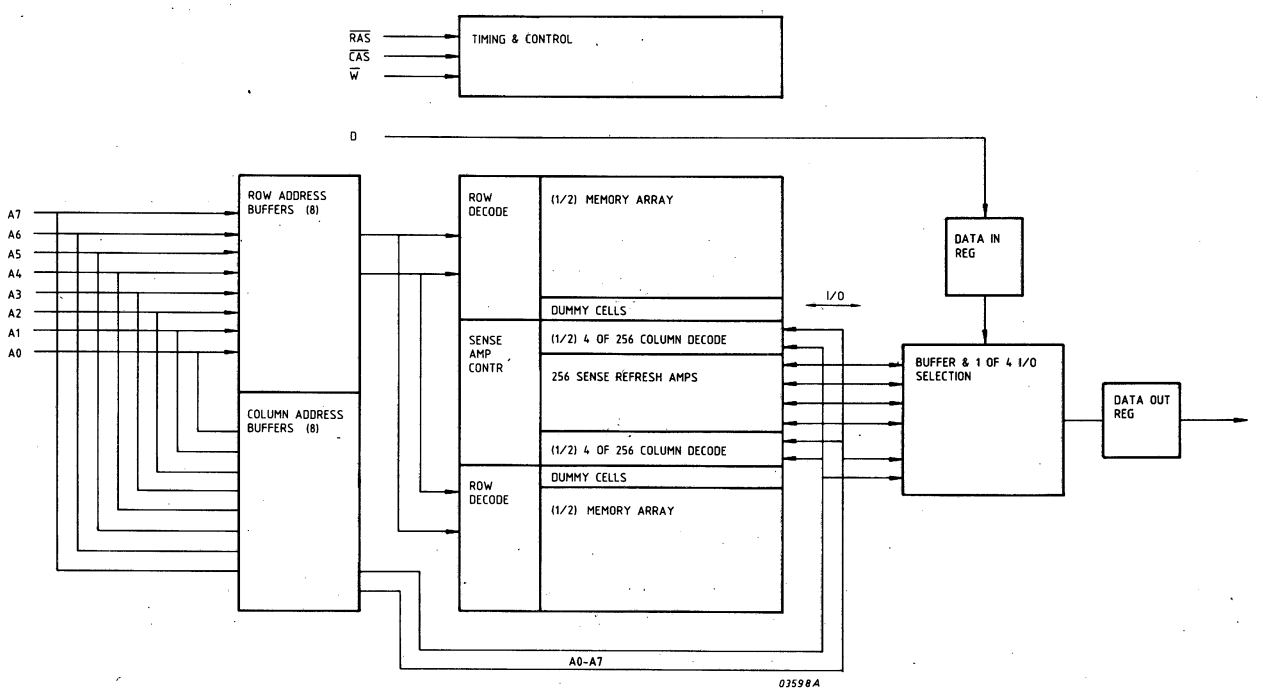


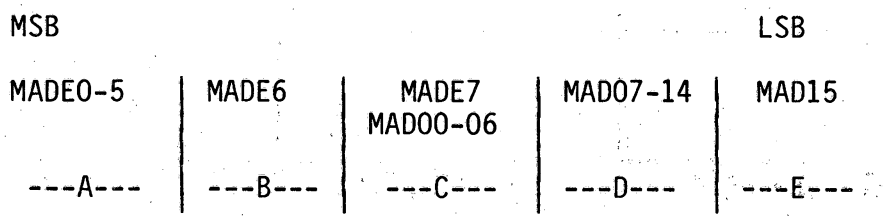
Figure 2.2 BLOCK DIAGRAM 4164-20

The memory cells in the memory device are organized as a matrix of 256x256 cells.
Sixteen address bits are required to decode 1 of 65.536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched into the chip by the row-address strobe (RASN). Then the eight column-address bits are set up on pins A0 through A7 and latched into the chip by the column-address strobe (CASN).

The read or write mode is selected through the write enable input. A logic high on the write enable (WEN) input selects the read mode and a logic low on the WEN input selects the write mode. Only those devices which received both RASN and CASN signals will execute a read or write cycle.
During the external cycle (read- or write cycle) only one bar is selected (left and right character) for a given address by the RASiN signal.
In a refresh cycle all two bars are selected (RASON - RAS1N).

2.2 MEMORY ADDRESSING

Addressing decoding is done for 24 bits of memory. These 24 bits are organized as indicated below.



A) MADE0 - MADE7

Memory Module Start Address Select Bits

This part of the address bits is used to locate the start address of memory module of 128K16 between 0 and 16M bytes in steps of 128K16.

B) MADE6

Is used to select one out of the two bars.

C) MADE7, MAD00 - MAD06

Are used to select the column address for the memory devices.

D) MAD07 - MAD14

Are used to select the row address for the memory devices.

E) MAD15

MAD15 is the character pointer, it will be used in the character mode only.
It indicates if the least or most significant octad (character) of the memory is directed to the least significant group of BI0N lines. (BI008N - BI015N).

2.3 DATA I/O

There are 6 possible Read/Write cycles.

The simplified diagrams are given in figure 2.3 till 2.8 with a short explanation of the data flow.

Figure 2.3 - Write Word
Figure 2.4 - Read Word
Figure 2.5 - Write Left Character
Figure 2.6 - Write Right Character
Figure 2.7 - Read Left Character
Figure 2.8 - Read Right Character

A memory cycle (Read or Write) will always read or write a complete word even in the character mode.
Word/character decoding logic and the character control logic are generating the desired control signals for the Data in/out latches and transceivers.

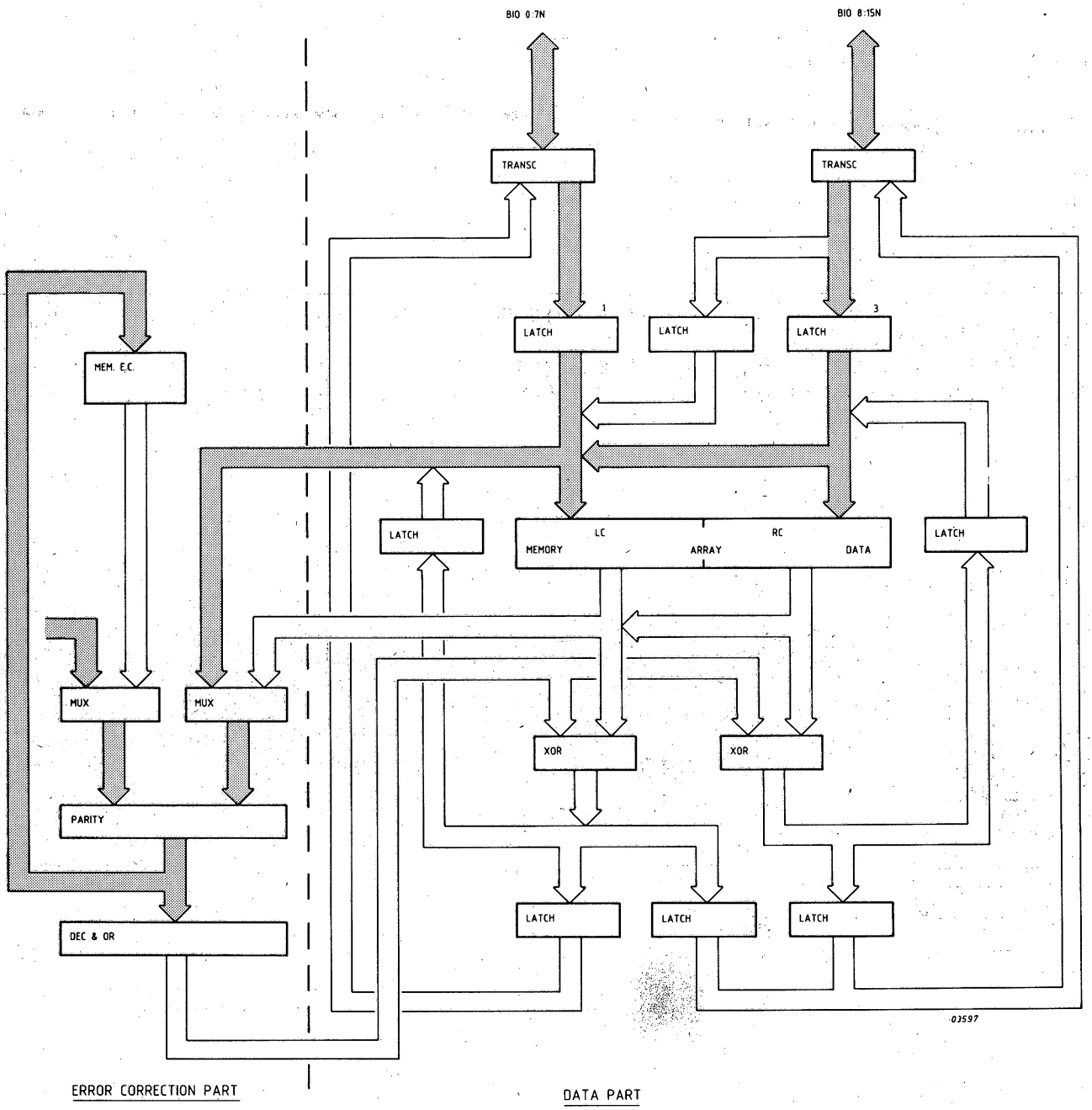


Figure 2.3 WRITE WORD

SIMPLIFIED DATA FLOW WRITE WORD.

Data on the BIO - N lines is latched in latch 1 and 3 and sent to the memory array to be written. The data latched is also sent to the error correction part to generate the right error correction code. The generated error correction code is written at the same time as the data into the error correction part of the memory.

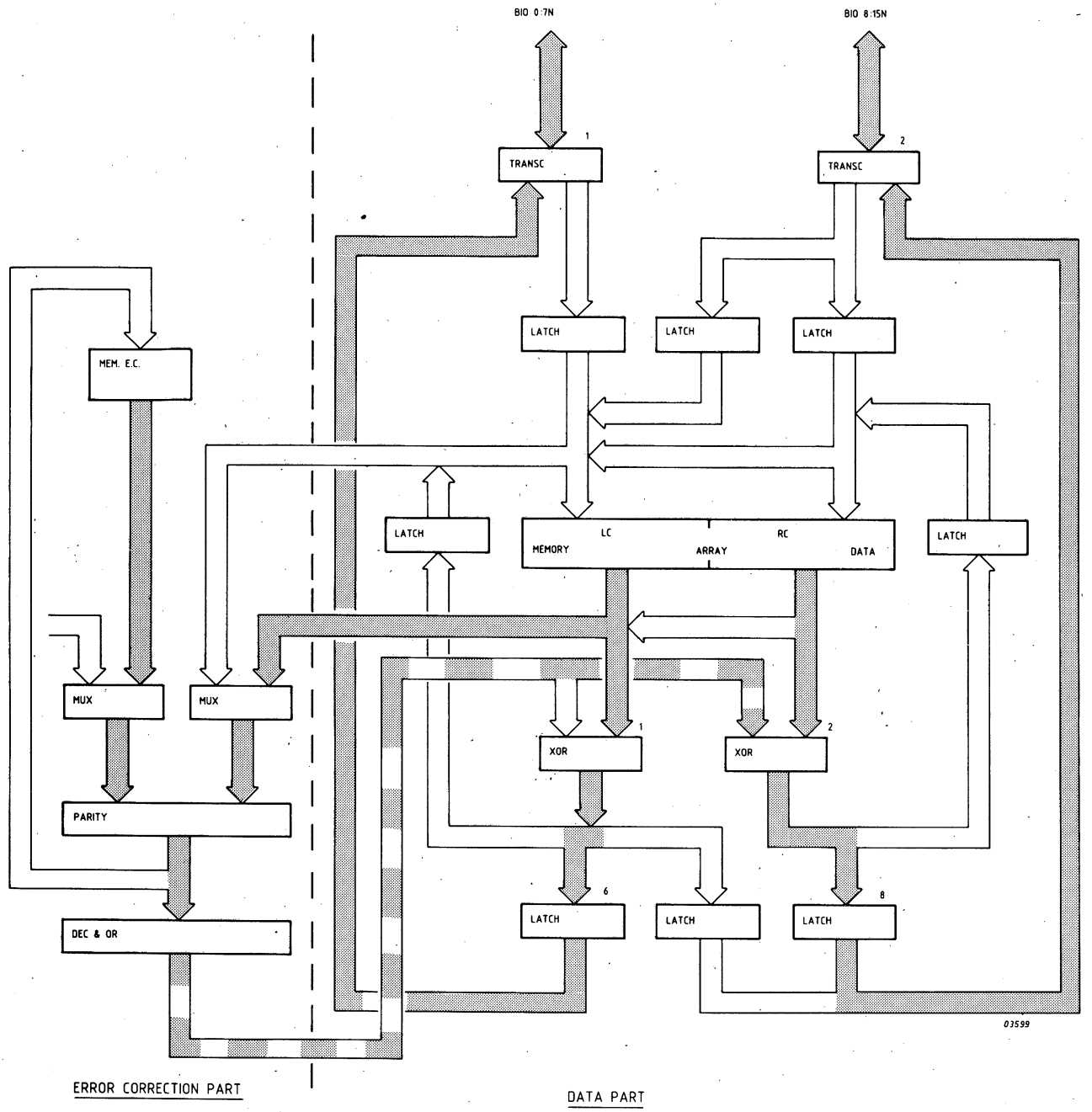


Figure 2.4 READ WORD

SIMPLIFIED DATA FLOW READ WORD.

The data read out during the read cycle is sent through the exclusive or-'s (XOR 1 and 2) and latched by LATCH 6 and 8. The latch data is set by the transceivers TRANSC 1 and 2 on the BIO-N lines.
During the read cycle the data from the memory array is also sent to the error correction part where it is combined with the error correction data (read out at the same time) to see if there is a single bit error.
In case of no error the decoder and or gates (DEC and OR) stay disabled so the output to XOR 1 and 2 (dotted line) is stable low; in case of an error the concerning bit is corrected by XOR 1-2 before the data is latched into latch 6 and

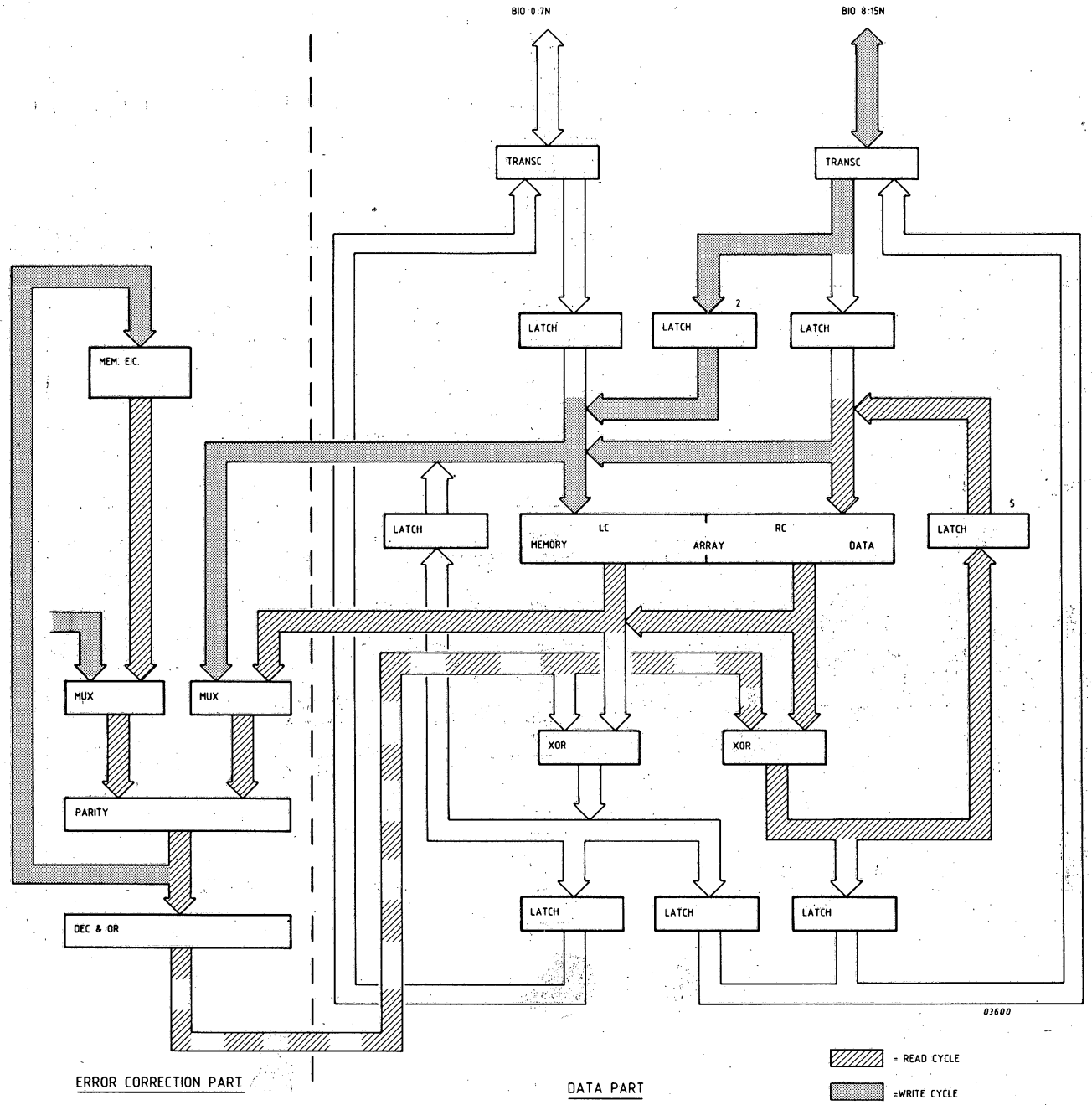


Figure 2.5 WRITE LEFT CHARACTER

SIMPLIFIED DATA FLOW WRITE LEFT CHARACTER.

In the character mode data transfer is always via BIO 8 : 15N. As the error correction bits are derived from a word one has to perform a read cycle before the write cycle to save (in this case) the data of the right character and to generate new error correction bits from the new left character data and old right character data.
In the same way as in a read word cycle. Left character data is latch into LATCH-2 the old right character data is in the read cycle latched into LATCH-5.

= Read cycle. = Write cycle.

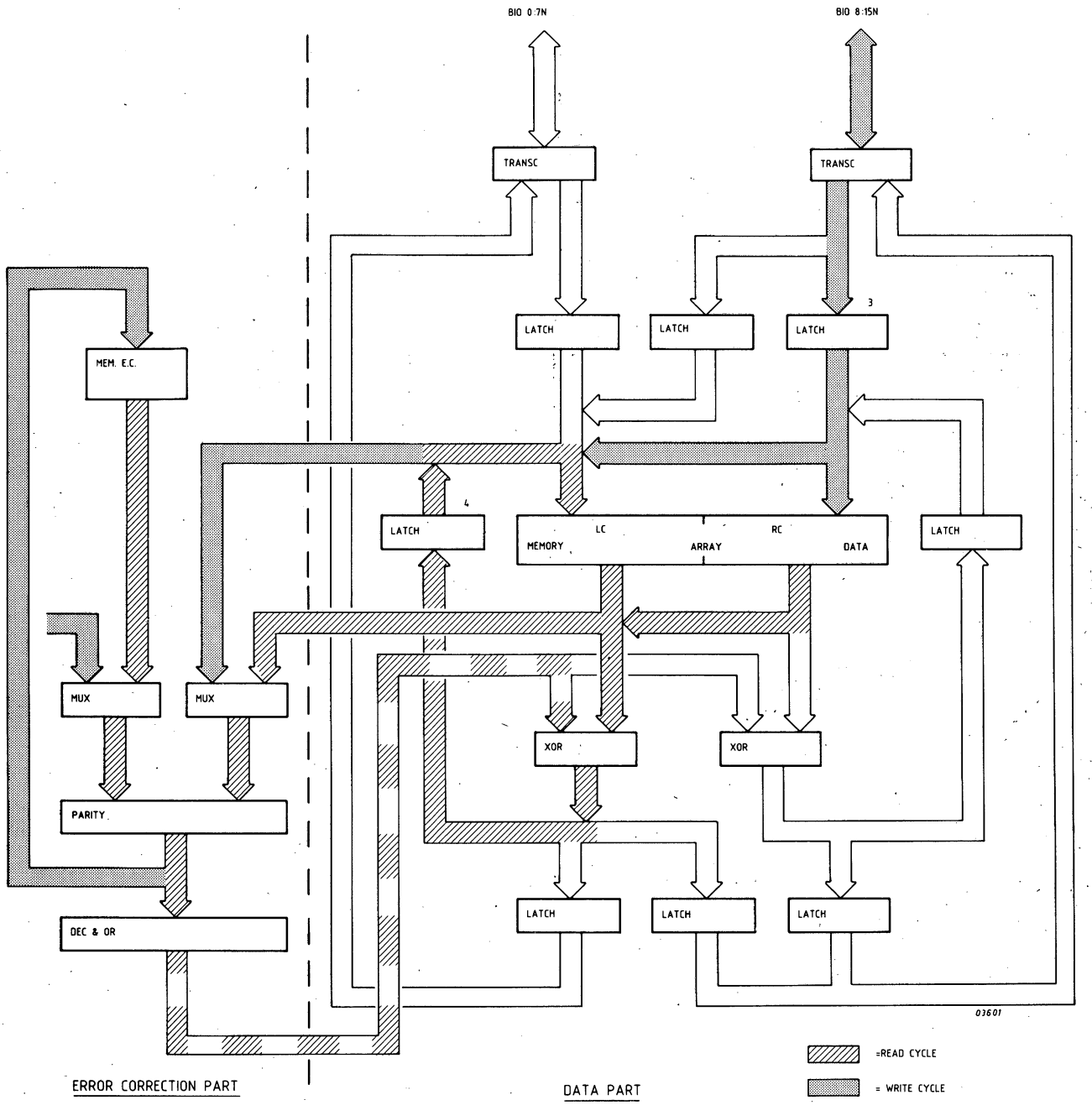


Figure 2.6 WRITE RIGHT CHARACTER

SIMPLIFIED DATA FLOW WRITE RIGHT CHARACTER.

The same as for write left character counts for write right character.
In this case the left character data has to be saved by a read action and latched into latch - 4.
The right character data is latched into latch - 3.

= Write cycle.

= Read cycle.

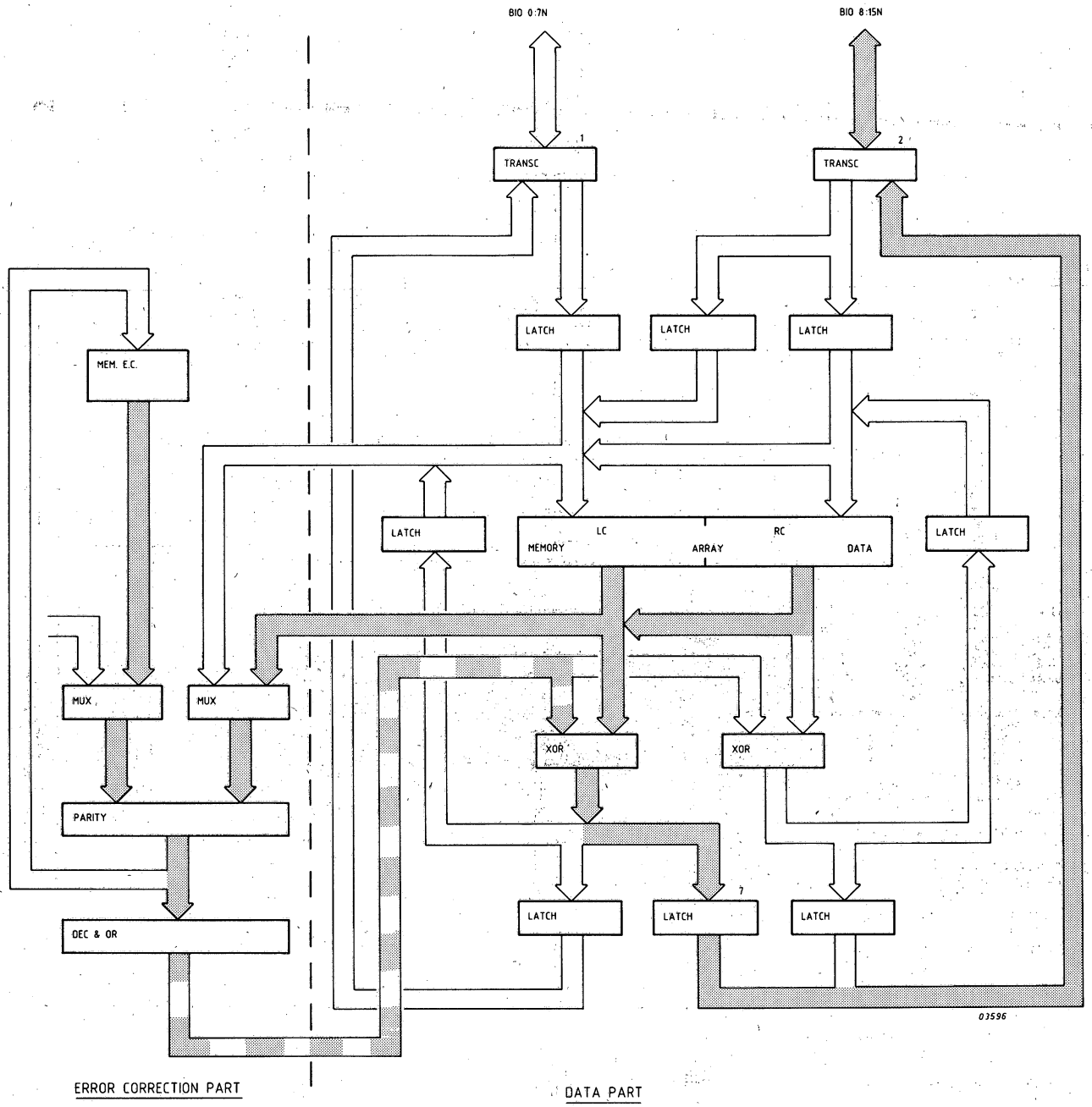


Figure 2.7 READ LEFT CHARACTER

SIMPLIFIED DATA FLOW READ LEFT CHARACTER.

Data transfer is in the character mode via BIO 8:15 N.
The transceiver TRANSC-1 is in the character mode to bus side (BIO 0:7N) always in the Hz-mode.
The data is read and corrected in the same way as in the read word mode, only the latches are enabled/disabled in such a way that only the left character data is set on the BIO-N lines.
Output data of the left character is latched into LATCH-7 and sent through TRANSC-2 to BIO 8-15 N.

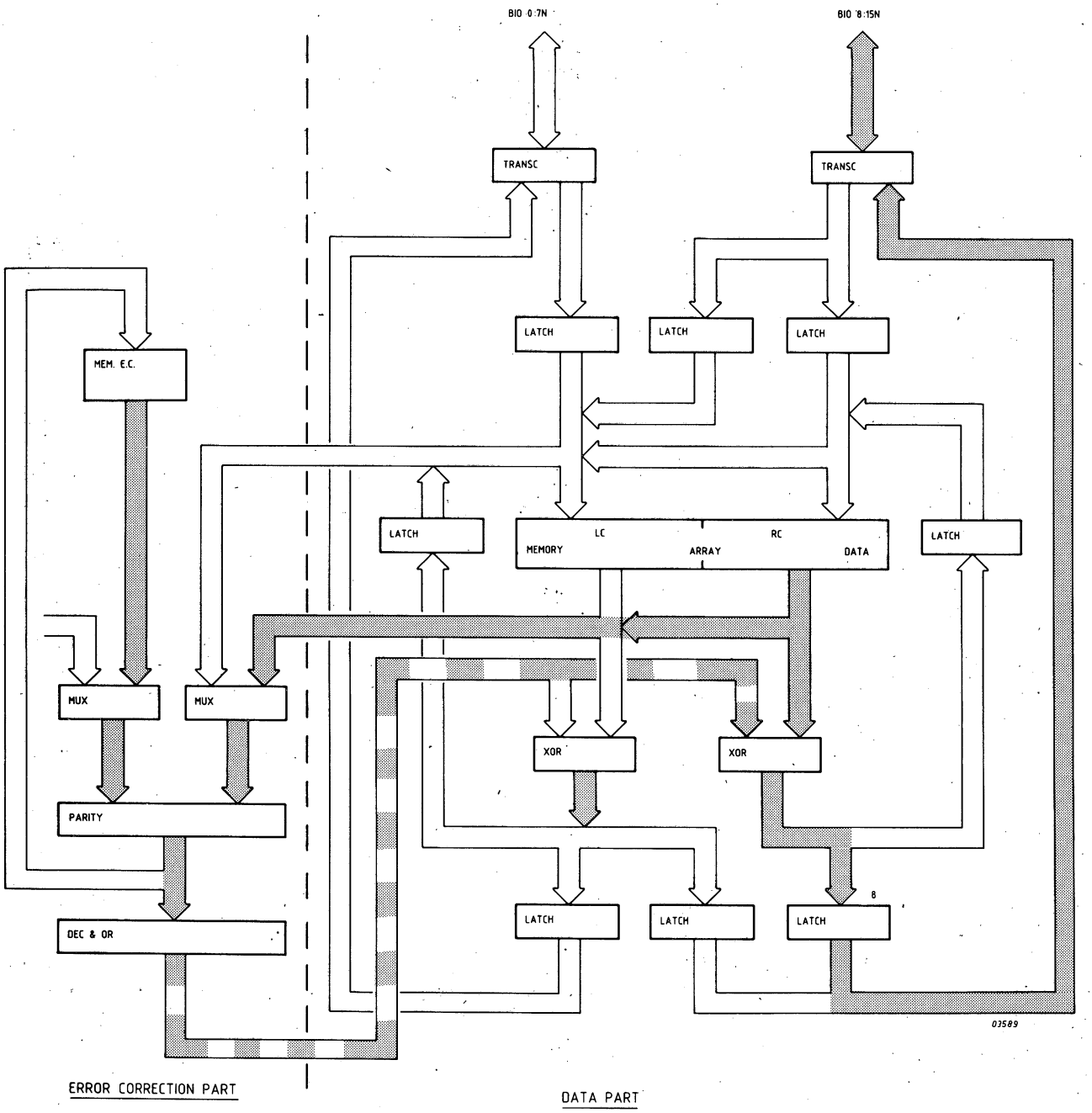


Figure 2.8 READ RIGHT CHARACTER

SIMPLIFIED DATA FLOW READ RIGHT CHARACTER.

Same actions as for Read Left Character, only data out is latched into LATCH-8.

2.4 REFRESH CYCLE

The memory shall perform a refresh cycle within each 15us.
If a request is given during this refresh cycle the memory will store this request and will perform the access cycle after the refresh cycle.
So the maximum read/write access is the normal read/write access plus a refresh cycle. This will be indicated by the TSMN and ACN signal. All inputs signals have to stay valid till ACN goes low.
Note that also ACN is influenced by a refresh cycle.

If during a read or write cycle a refresh cycle starts all output signals will stay unchanged until the normal end of the read or write cycle indicated by the rising edge of TMRN.

2.5 TIMING AND CONTROL

The folloing functions can be distinguished:

Arbiter, will choose between external requests (TMRN) and internal refresh requests (RFRQ). It also synchronizes the external requests with the internal clock oscillator.

The refresh circuitry, which is necessary due to the dynamic nature of the memory devices, consists of two parts:
1) REFRESH TIMER with a period time of 15 usec in each period one refresh cycle must take place in order to refresh all rows in a memory device within time.
2) REFRESH CONTROL, will ask for a refresh cycle, either hidden or automatic and controls the refresh cycle.
   At the end of the refresh cycle it increases the REFRESH ADDRESS GENERATOR (counter).

MEMORY CYCLE TIMER, General timing generator from which all cycle timing signals are derived.

MEMORY CYCLE MODE CONTROL, Three input signals. WRITE, CHA and MAD15 indicate the kind of memory cycle to perform.
They are LATCHED in and DECODED. The decoded outputs in conjunction with the general timing will create the signals necessary to control the Data (I/O BUS TIMING CONTROL).
These decoded signals are also used for CYCLE CONTROL (Read, Write cycle and word, character mode).

2.6 ERROR CORRECTION

The error correction circuit is word oriented, so you always should perform a read/write word even in character mode.
The generation of check bits is done during a write word cycle.
There are 5 check bits needed to discover and repair a 16 bits word for one failing bit.
The repared word is not stored back in the memory allocation.
For error detection the same logic is used as for check bit generation.

2.7 INFLUENCE OF THE REFRESH ON ACCESS AND CYCLE TIME

The refresh action is performed, as far as possible "hidden" to avoid too long access times to the Masters on the bus system, but it is ensured that all cells are refreshed within 4 ms (as required by the memory development specification).
A "hidden" refresh cycle means that the refresh cycle is executed immediately after the internal end of a read or write cycle, this means that a great part of the refresh cycle is performed during the end of the old cycle and the start of new read or write memory cycle.
A refresh cycle is requested by the memory once in every period of 15us.
If in this period of 15us a Read or Write cycle occurs, an "hidden" refresh cycle will be executed immediately after the Read of Write cycle. This "hidden" refresh cycle will only occur after the first Read or Write cycle in this 15us period.
This "hidden" refresh cycle adds 562 ns to the cycle time of the running cycle, or 562 ns max. to the access time of the next cycle.
When there has been no Read or Write request within the 15us period an "Automatic" refresh is performed at the end of this 15usec. period.
If during the "Automatic" refresh cycle a Read or Write cycle occures the sequence of cycles will be as follows:

"Automatic" refresh cycle
"Read or Write" cycle
"Hidden" refresh cycle.

This precedure will increase the access time by 0 - 625 ns and the cycle time by 625 to 1187 ns and, or the access time of the NEXT cycle by 0 - 562.

3 DETAILED DESCRIPTION

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3.1 MEMORY MATRIX

3.1.1 MEMORY ARRAY/DEVICES

As explained in section 2.1 the complete memory is organized as a 2 bars by 21 columns of 64K bits random access dynamic MOS read/write memory based on the TMS-4164-20 device.
Figure 2.2 gives a general block diagram of the TMS-4164-20 and figure 3.1 gives a more detailed block diagram.

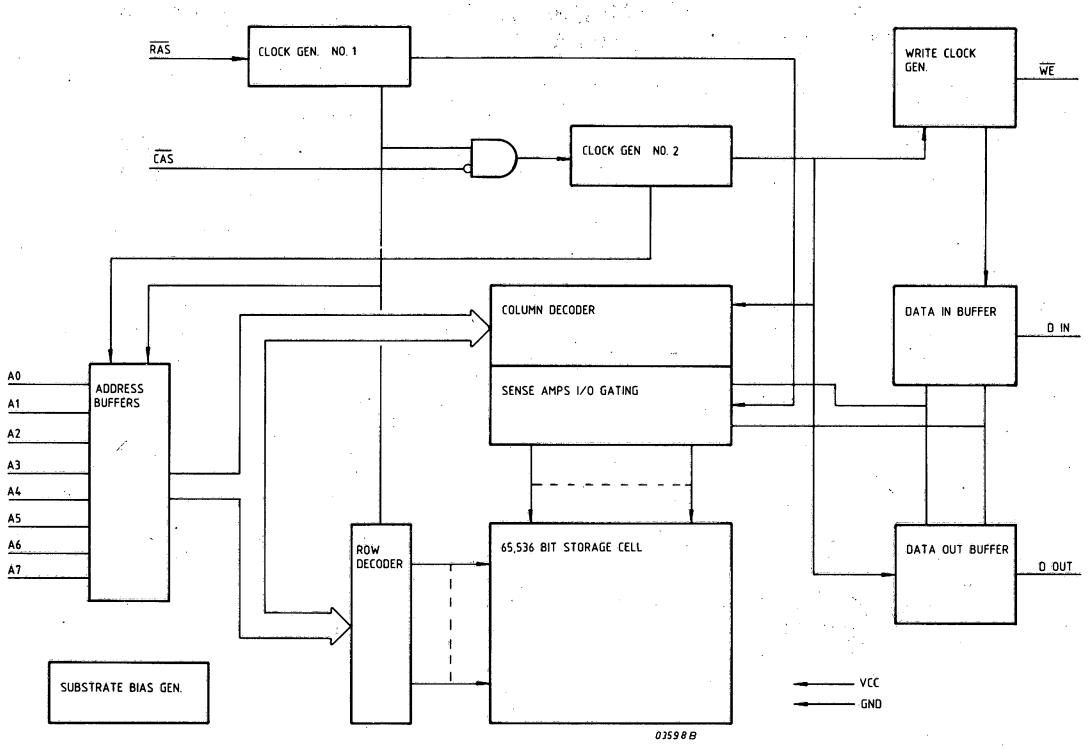


Figure 3.1 TMS-4164-20 DETAILED BLOCK DIAGRAM

3.1.2 ROW/COLUMN/WRITE ENABLE/ADDRESS DRIVERS

Figure 3.2 gives the memory with the drivers necessary.

The RAS/CAS and WE driver are separated for BAR0 and BAR1.
The address drivers are as well for BAR0 and BAR1.

RAS - Signals to the memory array are:
RANSON and RAS1N; input of the RAS drivers receive from the memory cycle timer signal RAS which determine the timing of RAS-N.
A decoded address bit gives this signals BAR0 and BAR1 as only one bar at a time can be accessed.

CAS - The CAS signal from the memory cycle timer goes to the drivers which give the signals CASON and CAS1N.
Only in a refresh cycle the CASON and CAS1N must not be given, so signal RFCYN is also sent to the CAS-driver.

WE - Timing for the WE-driver is T3 from the memory cycle timer and signal WCY is given to be sure that the signals WEN 0 and WEN 1 are only given during a WRITE - cycle.

ADDRESS - The address drivers consist of S158 multiplexer circuits, which are for as well BAR 0 and BAR 1.
Signals which are sent to the memory array are A0:7.
Input signals are ADL07/ADLE, ADL00/ADL08, ADL01/ADL09, ADL02/ADL10, ADL03/ADL11, ADL04/ADL12, ADL05/ADL13, ADL06/ADL14.

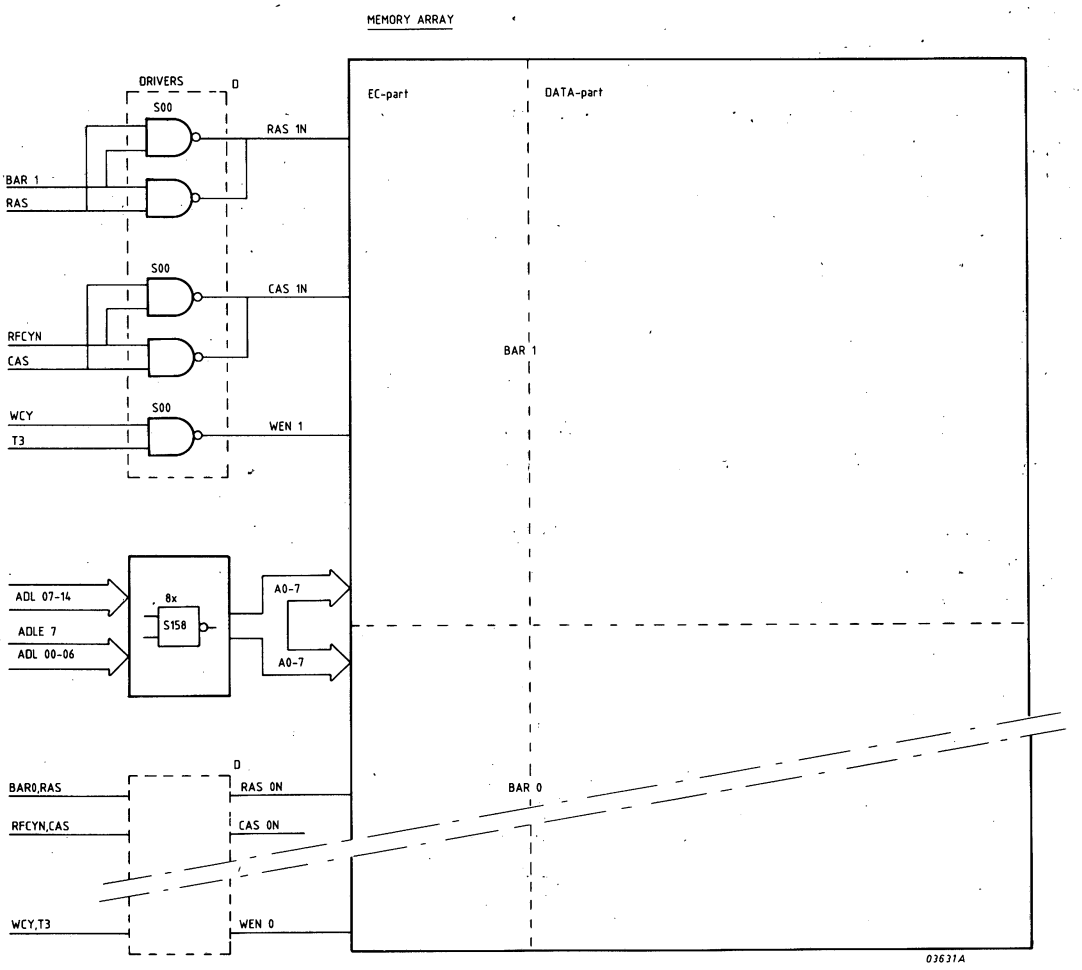


Figure 3.2 MEMORY ARRAY AND DRIVERS

3.2 MEMORY ADDRESSING

This part describes all address facilities concerning the module such as:
1. Module start address selection
2. Device address generation
   Refresh address generation

As already given in 2.2, 24 bits are offered to the memory module namely MAD00:15 and MADE 0:7.
This 24 address bits have an addressing capability of 16M.
Depending on the module capacity one can see in the list on the next page the function of the offered address bits.

a) 128K16:	MS							B	Y								X							C
b) 64K16:	MS								Y								X							C
c) 32K16:	MS								Y							B	X							C
MAD	E0	E1	E2	E3	E4	E4	E6	E7	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

MS = module selection address field
B = bar selection address bit
Y = column address for the memory devices
X = row address for the memory devices
C = character pointer.

MAD 15 is only active in the character mode see above so the addressing area is 16M byte or 8M words of 16 bits.

3.2.1 MODULE START ADDRESS SELECTION

The list given in 3.2 indicates which address bits are for module selection.
At the start of a memory request all memory modules present will latch the offered addresses.
Every module present has to compare the module selection address bits with the adjusted module start address to see if this memory request has to be handled or not.
As indicated below module selection address bits are latched by a LS373 and compared by a LS688. The adjustment takes place by means of plugs connected to logic "1" or "0".

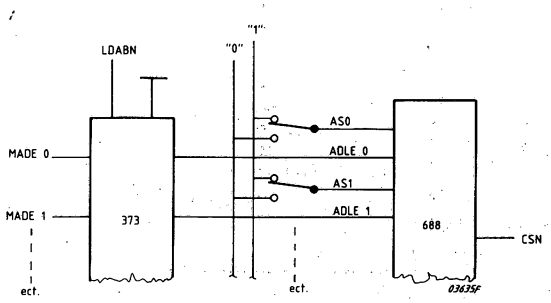


Figure 3.3 MODULE START ADDRESS SELECTION LOGIC

3.2.2 CAPACITY

Due to the universal design of this module some manipulations have to be done depending of the capacity/memory device used in the module.
There are 3 possibilities namely:
1. Complete module (128K16) using 64K dynamic RAMS.
2. Half populated module (64K16) using 64K dynamic RAMS.
3. Complete module (32K16) using 16K (5V only) dynamic RAMS.

As indicated in 3.2 some manipulations have to be done for module selection, BAR selection and memory device selection.

. Module start address.
  For a complete module (128K16) there are 6 module selection address bits and also 6 adjustment plugs available to place the module of 2^6 = 64 possible start addresses.
  It is easy to see that in case of a half populated module the number of module selection bits and adjustment plugs becomes 7.

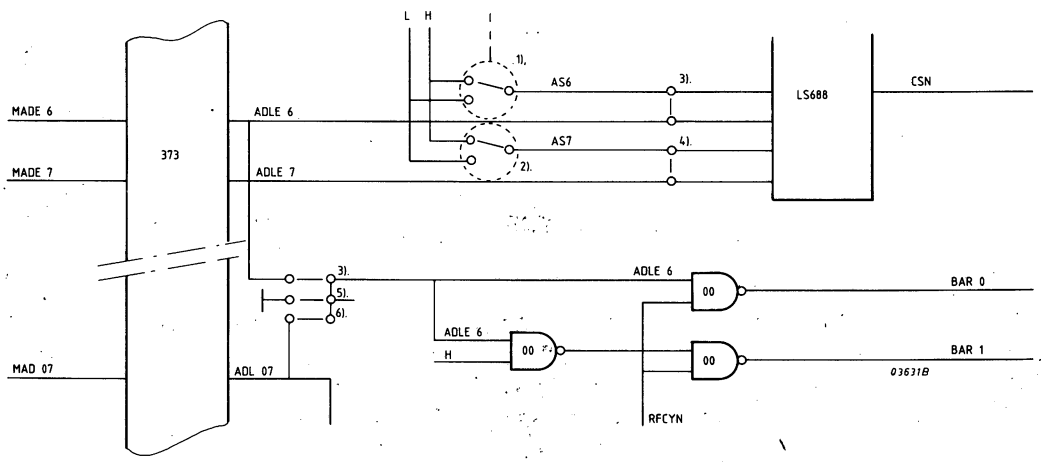
One more module selection bit and plug will be added in case of a 32K16 module.

. BAR selection
  As there are only two BARs, only for the complete module BAR selection takes place. For the 128K16 module BAR selection address bit corresponds with MADE 6 and for the 32K16 module with MAD 7.

. Device selection
  For the 64K dynamic RAM addresses are generated from MAD0:14 and MADE7; for the 16K RAM from MAD 0:6 and MAD 8:14.
  Below the 3 possibilities are given; the adjustments are done by means of "print path" - connections. (see figure 3.4).

CROSS TALK

Special attention has been paid to minimize cross talk between adjacent address lines in the memory matrix.



1) not placed for 128K16 module
2) not placed for 128K16 and 64K16 module
3) erase "print path" for 32K16 and 64K16 module
4) erase "print path" for 32K16 module
5) erase "print path" for 32K16 and 128K16 module
6) erase "pritn path" for 64K16 and 128K16 module

Figure 3.4 MODULE VERSION SELECTION LOGIC

3.2.3 DEVICE/REFRESH ADDRESS GENERAITON

As the dynamic RAMs need address information to select the rigth row and column the concerning address bits for row and column has to be multiplexed as the address input of the devices is common for row and column.
By selecting the right row and column the corresponding cell information of the device is set on the output in case of a read.
As we have dynamic RAMs the data stored has to be refreshed every 4 ms to keep it alive. Refreshing can be done to perform a read or RAS - only cycle.
As it is only necessary to do refresh cycles on rows, the row address bits for non-refresh cycle are combined with the refresh address bits as indicated in figure 3.5.
The refresh address is generated by means of LS393 which is incremented after every refresh cycle by means of RFCY.

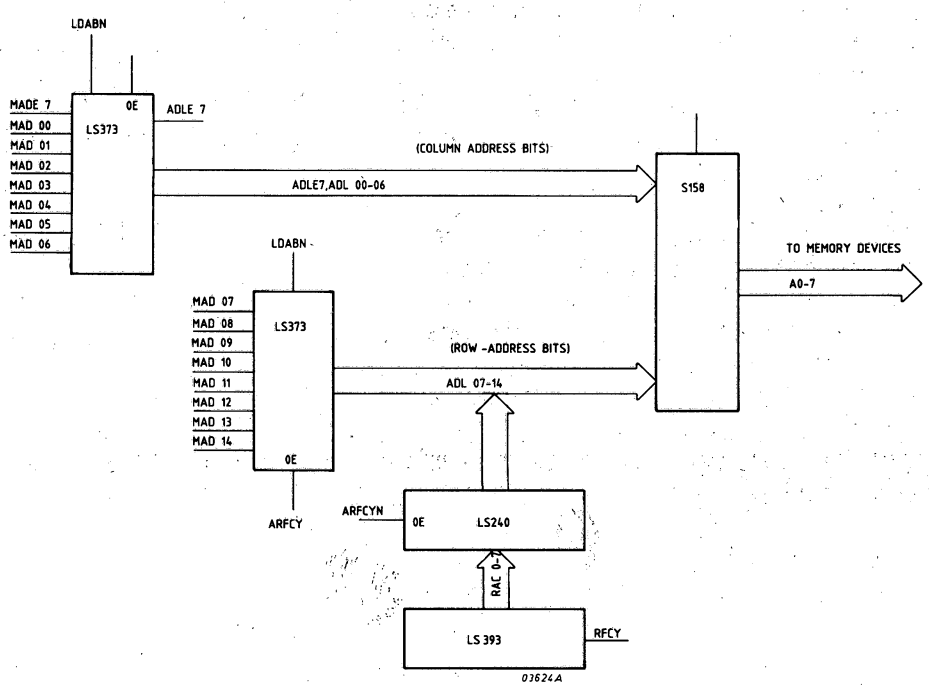


Figure 3.5 DEVICE REFRESH ADDRESS SELECTION

The refresh address RAC 0:7 becomes in case of a refresh cycle ROW-address as the LS240 is enabled by means of ARFCYN and the concerning LS373 is disabled by means of ARFCY. A refresh cycle is performed every 15us.
As the refresh address is 8 bits wide as well devices with 256/4 ms as devices with 128/2 ms are refresh in a proper way and time.
Multiplexing of the ROW and COLUMN address bits is done by S158 multiplexer circuits where the right timing is arranged by MX; output signals of the multiplexer go to the memory array.

3.3 DATA I/O AND CONTROL

3.3.1 GENERAL

At the moment a read or write request is accepted by the module some static signals will be sent till next read or write request takes place. There static signals are used to enable/disable the output of latches and/or set multiplexers in the right selection mode.
Some other signals which control the data flow are timed by the memory cycle timer.
In 2.3 the flow of the six possible Read/Write cycles are given.
In table 3.1 the state of the static and timing controlled control signals are given for these six possible Read/Write cycles.

3.2.2 UPL-INTERFACE

All data transport between UPL-bus and the module is done via transceivers 1 and 2 (4 x 8T26).
During a read in word mode the data outputs to the UPL-bus are enabled by the control signals TRDOL and TRDOR as long as TMRN is low.
In a write cycle all bus drivers are switched off and the transceivers act as a receiver for the incoming data.

3.3.3 MEMORY WRITE

The data which has to be stored is latched by the signal LDABN.
Left character is latched by latch-1, right character by latch-2 and 3. In the word mode output of latch-1 and 3 is enabled by means of CHAV and ERCHN. In the character mode latch-2 or 3 is enabled by means of ERCH and ERCHN, which one depends of it is a write left or right character, see table 3.1. Write in character mode is more complicated, as before the actual write a read cycle is necessary.
During the read cycle the character which has not to be written (old character) has to be saved and corrected if necessary. This old character is latched by means of LMDO in latch 4 or 5 depending on its being a left or right character. (See also data flow figure 2.3 and figure 2.8).
After this read cycle a new word is available which can be handled as data in a write word cycle.

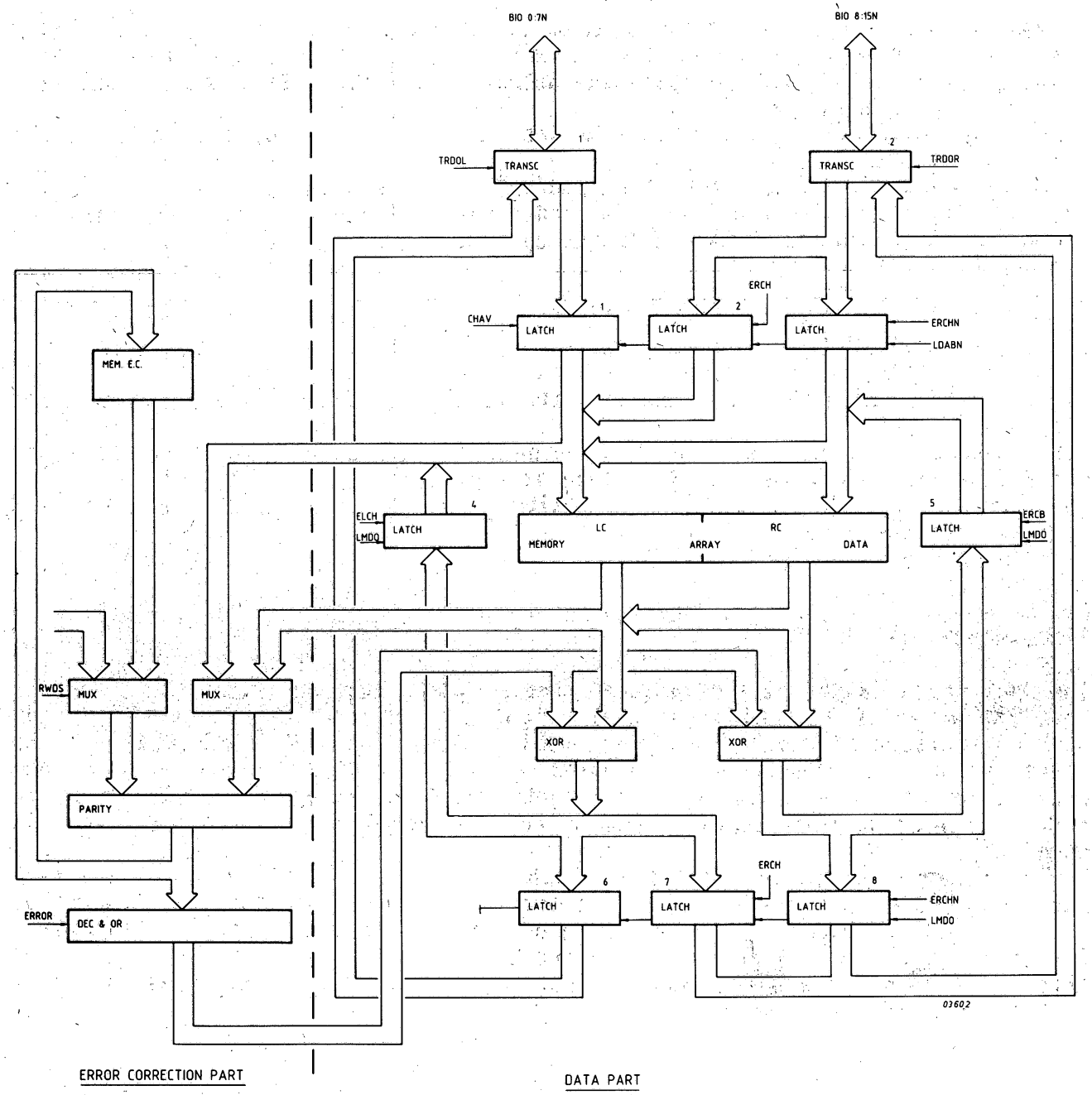


Figure 3.6 DATA I/O CONTROL

Signal	Read Word	Write Word	Read Left CHAR	Read Right CHAR	Write Left CHARACTER		Write Right CHARACTER	
					READ	WRITE	READ	WRITE
TRDOR	H(T3)	L	H(T3)	H(T3)	L	L	L	L
TRDOL	H(T3)	L	L	L	L	L	L	L
CHAV	L	L	H	H	H	H	H	H
ERCH	H	H	L	H	L	L	H	H
ERCHN	L	L	H	L	H	H	L	L
ELCH	H	H	H	L	H	H	L	L
LMDO	H(T3)	H(T3)	H(T3)	H(T3)	H(T3)	H(T3)	H(T3)	H(T3)
RWDS	H	L	H	H	H	L	H	L
ERROR	H(T3)*	X	H(T5)*	H(T5)*	H(T5)*	X	H(T5)*	X

* = in case of an error
X = don't care
() = signal time with signal between brackets

Table 3.1 STATE OF CONTROL SIGNALS FOR DATA I/O

3.3.4 MEMORY READ

The procedure for reading in the word or character mode is for both the same with the following exceptions:
. Transceiver TRANSC-1 is in the character mode (to bus side) always in high impedance.
. In case of read left character latch-7 is enabled and latch-8 disabled.

The output of the memory array (data part) is also sent to the error correction circuitry to check if there is a single bit error.
In case of an error signal ERROR becomes active and correction takes place.

All latches (1 : 8) are (S/LS)373 circuits.
XOR circuits for correcting a failing bit are (F/S/LS)86 circuits.

The decoder (2x(S/F)138) output in the error correction part stays stable high in case of no error ERROR = 0, so also the outputs of the OR-circuits (F/S)02 are stable now.

Note: (LS/S/F)XX; if the concerning circuits are LS, S or F circuits depends of the speed version of the module.

3.3.5 ERROR CORRECTION

The error correction circuit for this module is made by means of standard MSI and SSI TTL-'S in order to obtain a fast module with respect to access and cycle time.
For minimizing the number of TTL-'s in the error correction part the same parity circuits 5x74(LS/S/F)280 are used for check bit generation in a write cycle and for Syndrome bit generation in a read cycle.
Figure 3.7 gives a simplified diagram of the error correction part.

Explanation of the error correction circuit during:

WRITE CYCLE

During the write cycle the data which has to be stored in the memory (MDI 00;15) is also sent to the error correction circuit to generate check bits. When these check bits are formed, they are stored at the same time as the concerning data and at the same address. The generated check bits form a code which is used during a read cycle to detect single bit failures and correct them.

In a write cycle signal RWDS is set in such a way that the data input MDI 00:15 is sent through the multiplexer (MUX) consisting of (LS, S, F)157 circuits to the parity circut. After the multiplexer the data-in bits are called ECD 00:15. Beside the signals ECD 00:15 the parity circuit received also the signals ECD S0:4. These are the stored check bits but in the Write cycle the signals indicated in figure 3.7 with *. These signals are during a write cycle always logic zero only for test purposes these signals (* = TSBIT 0:4) can have a value other than logic zero.
So the parity circuit build up from (LS, S, F)280 circuits received in a write cycle the signals ECD S0:4 (always "0") and the memory data-in ECD 00:15.
Check bit generation is done by generating parity bits over different groups of data in accordance with what is called a "modified" Hamming code.
As the check bits have to be generated from the data-in bits (ECD 00:15) only, this is the reason that ECD S0:4 has to be always "0".

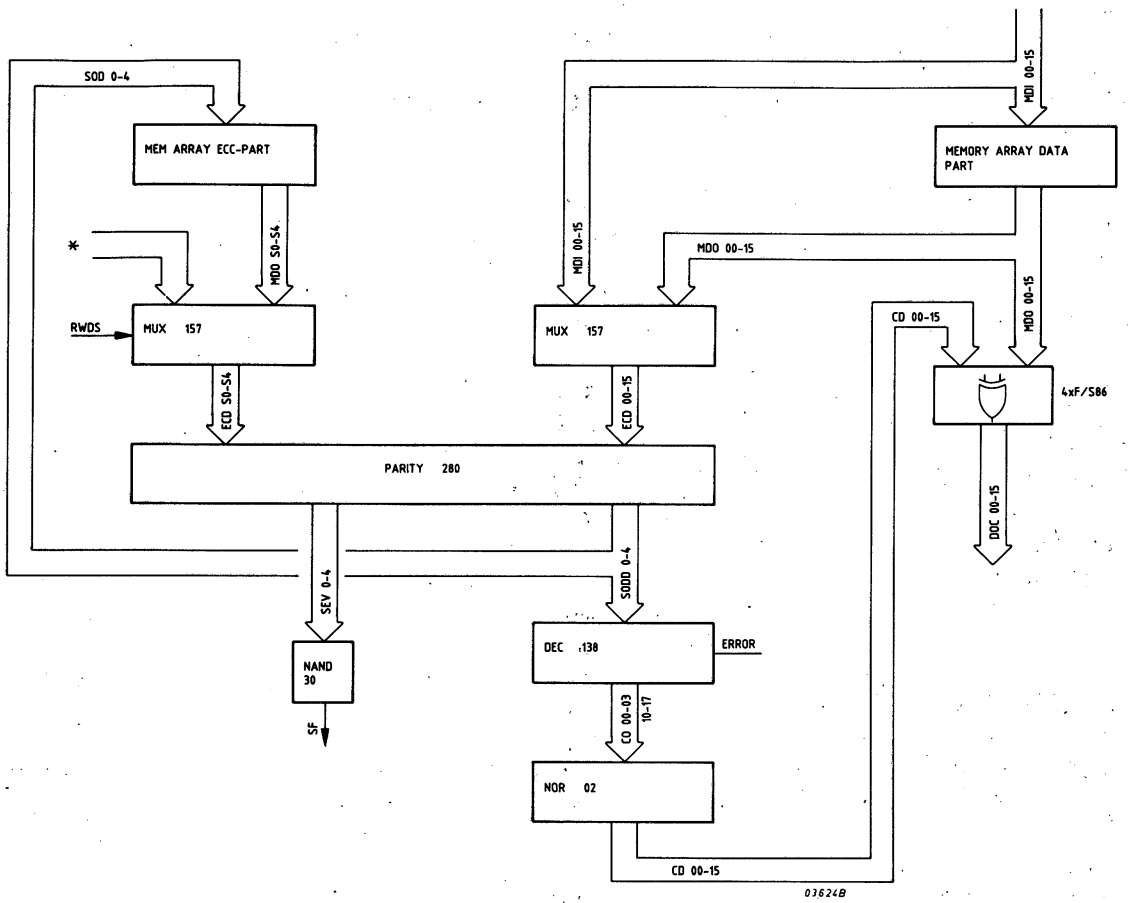


Figure 3.7 ERROR CORRECTION LOGIC

The check bits are generated by the following equation:

SODD0 = ECD00xECD01xECD02xECD03xECD04xECD05xECD06xECD07
SODD1 = ECD00xECD01xECD02xECD06xECD10xECD11xECD13xECD15
SODD2 = ECD00xECD03xECD09xECD11xECD12xECD13xECD14xECD15
SODD3 = ECD01xECD03xECD04xECD05xECD08xECD12xECD13xECD14
SODD4 = ECD02xECD04xECD07xECD08xECD09xECD10xECD14xECD15

x: exclusive ored.

SODD = Sigma odd parity.
Note that other output signals of the parity circuit are SECO:4 where SEVX = SODDX (X = 0:4).
The generated check bits SODD 0:4 are sent to the memory array (ECC-part) and stored at the same time and address where the corresponding data is stored.

READ CYCLE

See figure 3.7.
During the read cycle the data read out has to be checked on single bit errors and corrected if so.
The read out data (MDO 00:15) is sent through 4x74(F/S)86 circutis to the data out latches (DOC 00:15).

As in case of no error CD 00:15 are always logic zero; the data to the latches (DOC 00:15) corresponds with MDO 00:15 as the function of the (F/S)86 circuits is : DOCX = MDOX + CDX (X = 01:15).
In case of a single bit error one of the CD-bits will become logic "1" with the result that the concerning data bit is inverted by the (F/S)86 circuit and in this way corrected.
In which way the right CD-bit is set is described further on.
In the read cycle signal RWDS on the multiplexer circuits is set in such a way that signals MDO 00:15 (data out) and MDO S0:4 (check-bits) are sent to the parity circuit consisting of (LS, S, F)280 circuits as ECD 00:15 and ECD S0:4.
Now a new odd and even parity is formed (SODD 0:4 and SEV 0:4); now ECD S0:4 are not all "0" as in the write cycle, but are the generated check bits of the write cycle.
This new parity code now called syndrome-code is "0" (SODD 0:4 are all "0" and SEV 0:4 are all "1") in case of no error.
A single bit error will result in a certain syndrome code "0". This code has to be decoded to point to one of the data bits.
Table 3.2 gives the check bit generation;
Table 3.3 the data and check bit position in the encoded word of the modified Hamming chart and table 3.4 the syndrome bit decodation by the (S, F)138 circuits.

MDO :	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	(ECD 00:15)
SODD 0 =	x	x	x	x	x	x	x	x									
SODD 1 =	x	x	x				x				x	x		x		x	
SODD 2 =	x			x						x		x	x	x	x	x	
SODD 3 =		x		x	x	x			x				x	x	x		
SODD 4 =			x		x				x	x	x	x			x	x	

Table 3.2 CHECK BIT GENERATION

BINARY BIT:		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DATA-CHECK BIT:			S0	S1	06	S2		11	0	S3	05		01	12	03	13		S4	07	10	02	09		15		08	04			14			
	0	x		x					x		x		x		x				x		x						x						
	1		x	x				x	x		x		x			x				x	x			x									
SIGMA	2					x		x	x					x	x	x						x		x						x			
	3									x	x		x	x	x	x											x	x			x		
	4																	x	x	x	x	x		x			x	x			x		

Table 3.3 DATA AND CHECK BIT POSITION IN THE ENCODED WORD
MODIFIED HAMMING CHART

SYNDROME BITCODE	SODD 2		0	0	0	0	1	1	1	1	
	SODD 3		0	0	1	1	0	0	1	1	
	SODD 4		0	1	0	1	0	1	0	1	
SODD 0 - 1		C	10	11	12	13	14	15	16	17	output of S/F138-1)
0	0	0	NE	S4	S3	08	S2	09	12	14	
0	1	1	S0	10			11	15	13		
1	0	2	S1	07	05	04			03		
1	1	3	06	02	01		00				

output of S/F138-2 Bit in error, only data bits errors are corrected
NE = No Error

Table 3.4 SYNDROME BIT DECODING

From table 3.4 it is easy to see that the syndrome bit decodation output of the (S/F)138 decoders combined with a NOR-circuit (S/F)02 completes the decodation. Output of this NOR-circuits CD 00:15 are sent to the XOR circuits (F/S)86 where in case of an error the concerning bit is corrected.
The even syndrome bit output of the parity circuit SEV 0:4 (which are all "1" in case of no error) are sent to a NAND circuit 74S30 to generate signal SF.
In case of an error SF = 1.
To prevent decoding glitches on the data which is already driven on the UPL-bus, the decoder outputs are disabled by signal ERROR until SF is valid. In case of no error SF = 0 signal ERROR stays zero with the result that the decoder stays disabled.
A read cycle with correction takes some additional time and that is why the complete cycle is stretched (access and cycle time).

3.4 TIMING AND CONTROL

3.4.1 OSCILLATOR

The clock circuit of the module is a hybrid X-tal oscillator. It's oscillation frequency depends of the speed version of the module; for the standard speed version f = 16MHz, for the medium speed version f = 24*MHz and for the high speed version f will be 27.778*MHz.
Before used the oscillator output is buffered by two dotted OR-ed 74S00 circuits. See figure below.

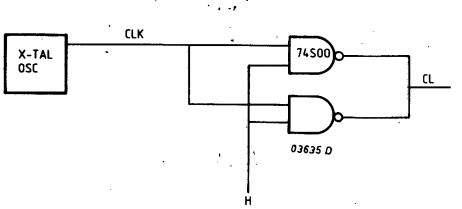


Figure 3.8 OSCILLATOR

* exact frequency not yet defined.

3.4.2 ARBITER

The function of the arbiter is to handle all memory requests and control signals in a proper way.
Memory requests can be:
. external : read or write request by an of TMRN
. internal : refresh request
External control signal is RSLN which indicates the state of the power supplies. Also external requests have to be synchronised with the internal clock which control the whole timing of the module.
Below simplified diagram of the arbiter is given.

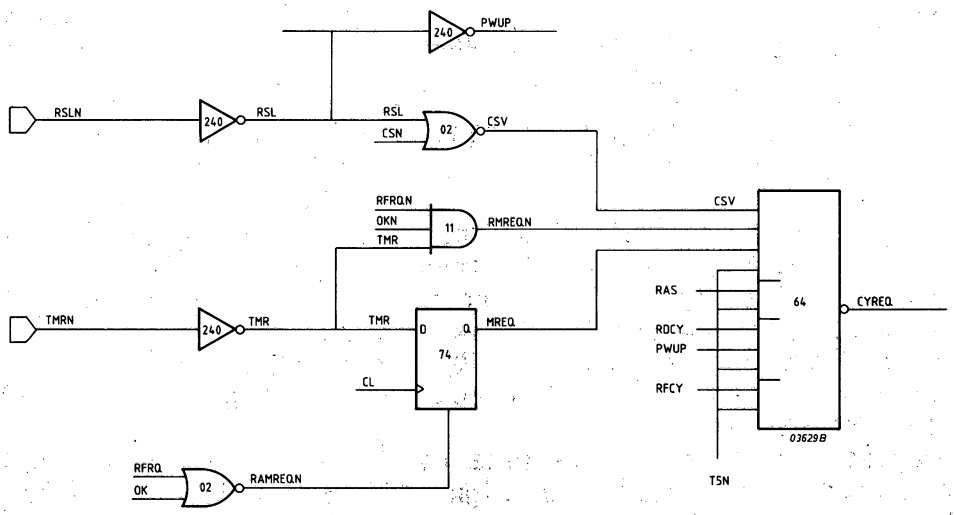


Figure 3.9 THE ARBITER

The start of a cycle (Read, Write or Refresh) is indicated by signal CYREQN which becomes low as a memory cycle has to be performed.

$$\overline{CYREQN} = \underbrace{CSV.RMREQN.MREQ.T5N}_{1} + \underbrace{RAS.T5N}_{2} + \underbrace{RDCY.PWUP.T5N}_{3} + \underbrace{RFCY.T5N}_{4}$$

The input conditions on the AOI (and or invert) 74S64 can be separated into four separate parts each with it's own function. If one of the conditions 1 till 4 is "1", CYREQN = 0 so a memory cycle can be activated.

1 CSV.RMREQN.MREQ.T5N
This part is the enterance of a read/write request by means of TMRN.CSV as to be "1" which indicates the request is meant for this module; RMREQN and MREQ become "1" as a request is applied to the module (TMRN to "0"); T5N which becomes "0" during the request cycle ensures that no cycle request can be started till it is "1" again.

2 RAS.T5N
This is a busy condition; if this equation becomes "1" the memory cycle timer is started and locked till this condition becomes "0" again.

3 RDCY.PWUP.T5N
Only active in the write character mode RDCY becomes "1" because a double cycle has to be performed (read before write cycle). The second cycle (write cycle) is directly initiated by this equation as the first one is finished.

4 RFCY.T5N
Initiation of a refresh cycle as RFCY becomes "1".

3.4.3 MEMORY CYCLE TIMER

This part of the module generates all timing signals to perform a right memory cycle including control signals for I/O, character and handshake.
Below circuitry and timing diagram is given.

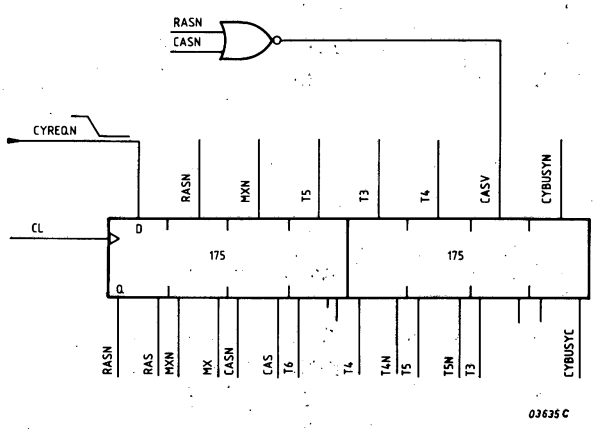


Figure 3.10 MEMORY CYCLE TIMING

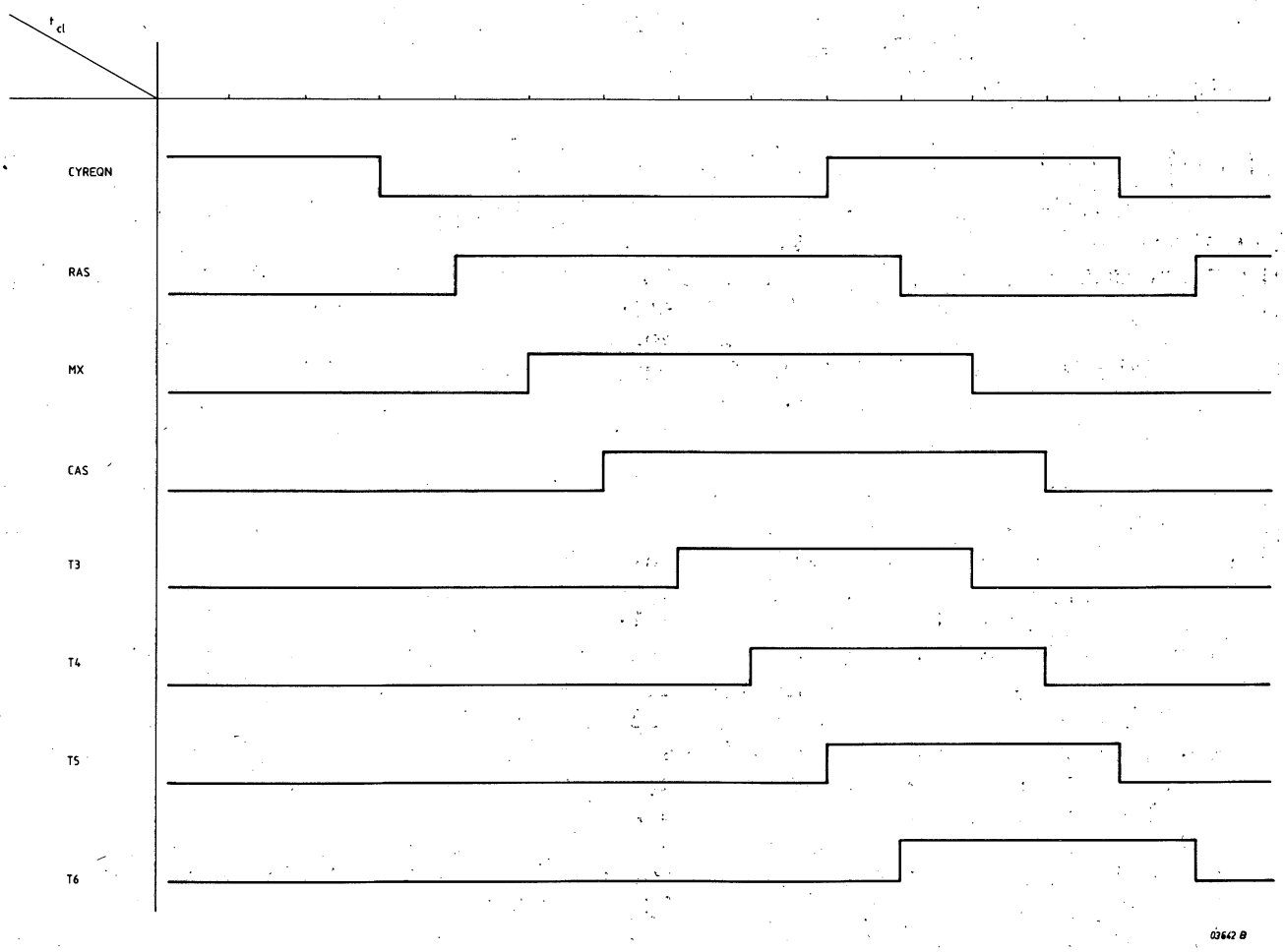


Figure 3.11 TIMING DIAGRAM MEMORY CYCLE

The timing signals are generated by two 74(S/F)175 quad D-flip-flops arranged as a shift register.
Input of the shift register is CYREQN and becomes "0" as a request has to be handled.
Schematics and timing diagram are clear enough to see how the timing signals are generated including the trick to generate T3.
For (worst case) timing reasons the signals of the two 74(S/F)175 circuits are divided as indicated.

With these signals all other signals necessary are generated.
Generation of CYBUSYC from CYBUSYN will be discussed further on.

3.4.4 REFRESH TIMER/CONTROLLER

The function of this part is to generate a refresh cycle so the data stored into the memory will stay alive.
To be in time, every row-address has to be accessed within 2 or 4 ms (depending of the memory device chosen) which results in an average time between two (ROW-address) refresh accesses of 2/128 or 4/256 which is 15.625us.
Some counter stages clocked by the oscillator signal CL will generate signal STRF which period has to be less than or equal to 15.625us. (see figure 3.12 and figure 4.3).
As this module is designed for some speed versions adjustments b.m.o. print-path connections has to be made. Beside the standard clock frequency of 16MHz., also clock frequencies of 24MHz* and 27.778MHz* has to be possible.

* = frequency not yet defined.

3.4.4.1 REFRESH REQUEST GENERATION

To fulfil the requirement of a refresh period of less than or equal to 15.625us for all speed versions following adjustments can be made (see figure 3.12);
a. first counter state (S175) /2 can be skipped.
b. last counter state (LS393) three combinations can be made
   - / 15
   - / 11
   - / 13

Note: /indicates divide by
16.000MHz : Clock period = t_{CL} = 62.5 ns
Present interconnections: b, c, d
Result: t_{STRF} = 62.5 x 16 x 15 ns = 15us
24.000MHz : Clock period = t_{CL} = 41.7 ns
Present interconnections: a, c, e
Result: t_{STRF} = 41.7 x 2 x 16 x 11 = 14.7us
27.778MHz : Clock period = t_{CL} = 36 ns
Present interconnections: a, d, e
Result: t_{STRF} = 36 x 2 x 16 x 13 = 14.98us

Signal STRFN is set on the clear input of the last couterstage to generate a /15 (for 16MHz), a /11 (for 24MHz) and a /13 (for 27MHz).

3.4.4.2 TIMING REFRESH PART

Figure 3.11 gives the diagram of the refresh part.
One can distinguish the following funcitions:

i. a refresh request has to be generated every 15us.
ii. the generated refresh request has to:
    a) set the hidden refresh request flip-flop if not set yet.
    b) initiate an automatic refresh if the hidden refresh condition is still present.
iii. generating of an advanced refresh request which will block read or write requests.
iv. generating of signals for a proper refresh cycle.

Ad.i. Figure 3.13 gives the timing diagram of the generation every 15us of STRF. The leading edge of STRFN initiates an automatic refresh as RFRQH=1 (already set by a previous STRF puls).
The trailing edge of STRF always set the hidden FF (LS74) to RFRQH=1.

3.4.4.3 AUTOMATIC REFRESH

If there is no read/write request during a 15us period between two "STRF pulses" then a refresh is performed at the end of the 15us period. This is called an Automatic Refresh (A.R.).

3.4.4.4 HIDDEN REFRESH

If there is a read/write request during a 15us period between two "STRF pulses" then a refresh is performed immediately after the first (AND ONLY THE FIRST) read/write cycle.
This is called a Hidden Refresh (H.R.) because the refresh can usually be performed before the master can respond to the TSMN and reactivate the TMRN for another read/write cycle. When the memory is busy, therefore the chance of a master having to wait for the memory to perform a refresh is negligible.

In figure 3.12 the hidden refresh request FF (output RFRQH) and the automatic request FF (output ERFRQ) are indicated with [ ].
The hidden -FF is set by STRF and can only be reseted (b.m.o. RRFRQHN) as the refresh was initiated by a read or write request.
An automatic refresh is initiated by STRFN by making ERFRQ active; requirement is of course that RFRQH=1.
The pre-actions, for a refresh cycle, start as EARFRQN becomes active.

$$\overline{EARFRQN} = \underbrace{RFRQH.T3.}_{I}\ \underbrace{\overline{T5N.RFCYN}}_{II}+\underbrace{ERFRQ.RFCYN}_{III}+\underbrace{\overline{RFCY.ARFRQ.MXN}}_{IV}+\overline{ARFRQ.RFCYN}$$

Figure 3.14 gives the timing diagram of a refresh cycle initiated by an automatic refresh request.
ERFRQ become "1" as result of STRFN and RFRQH=1 (hidden refresh request was waiting to be handled).
EARFRQN becomes active as part II eq. (1) becomes "1".
One clock period later ARFRQ =1 and will create a lock as part IV of equation (1) becomes "1". This locked situation can only be interrupted as the actual refresh cycle is started (RFCYN becomes "0").

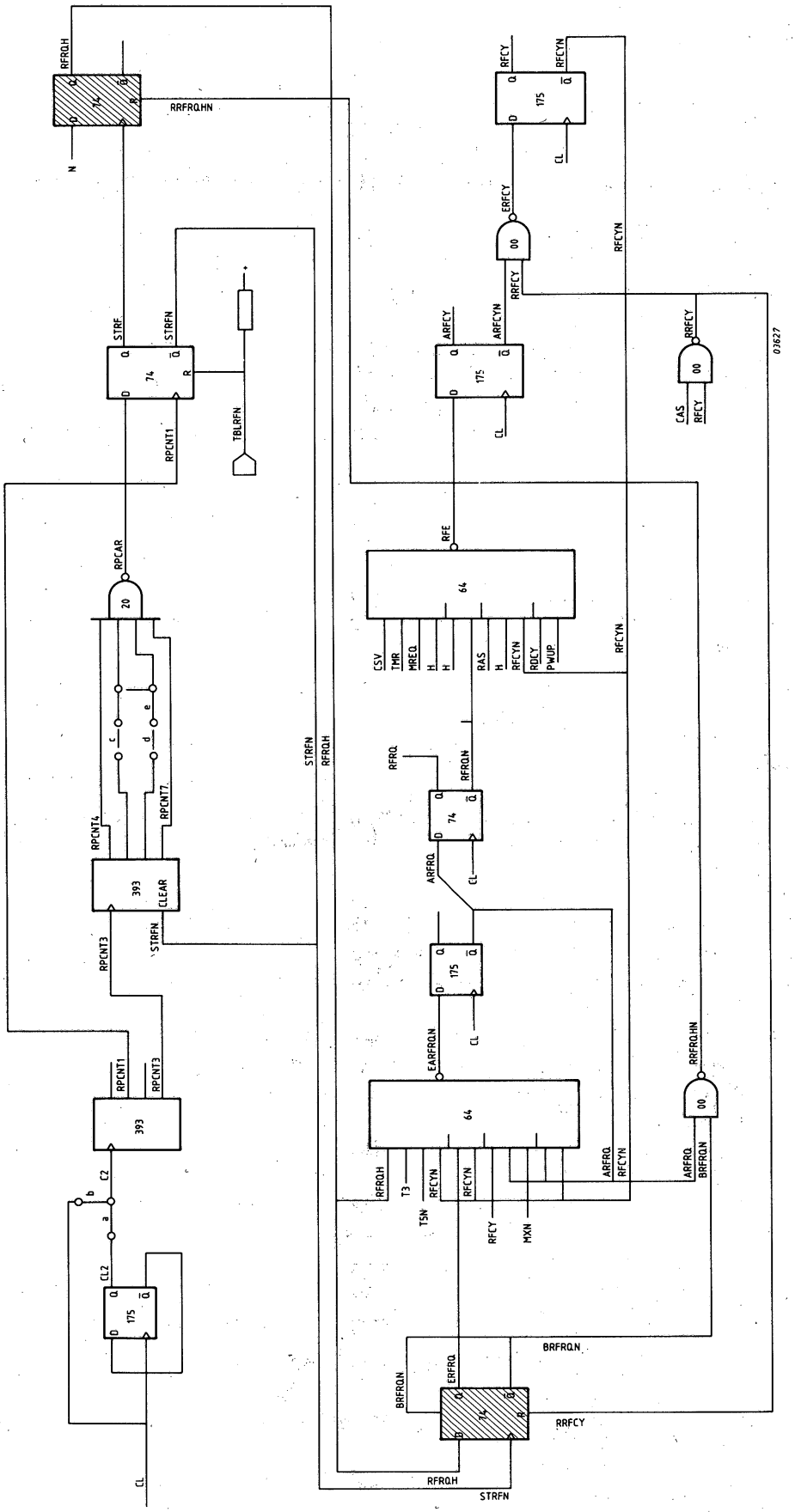


Figure 3.12 DIAGRAM OF THE REFRESH PART

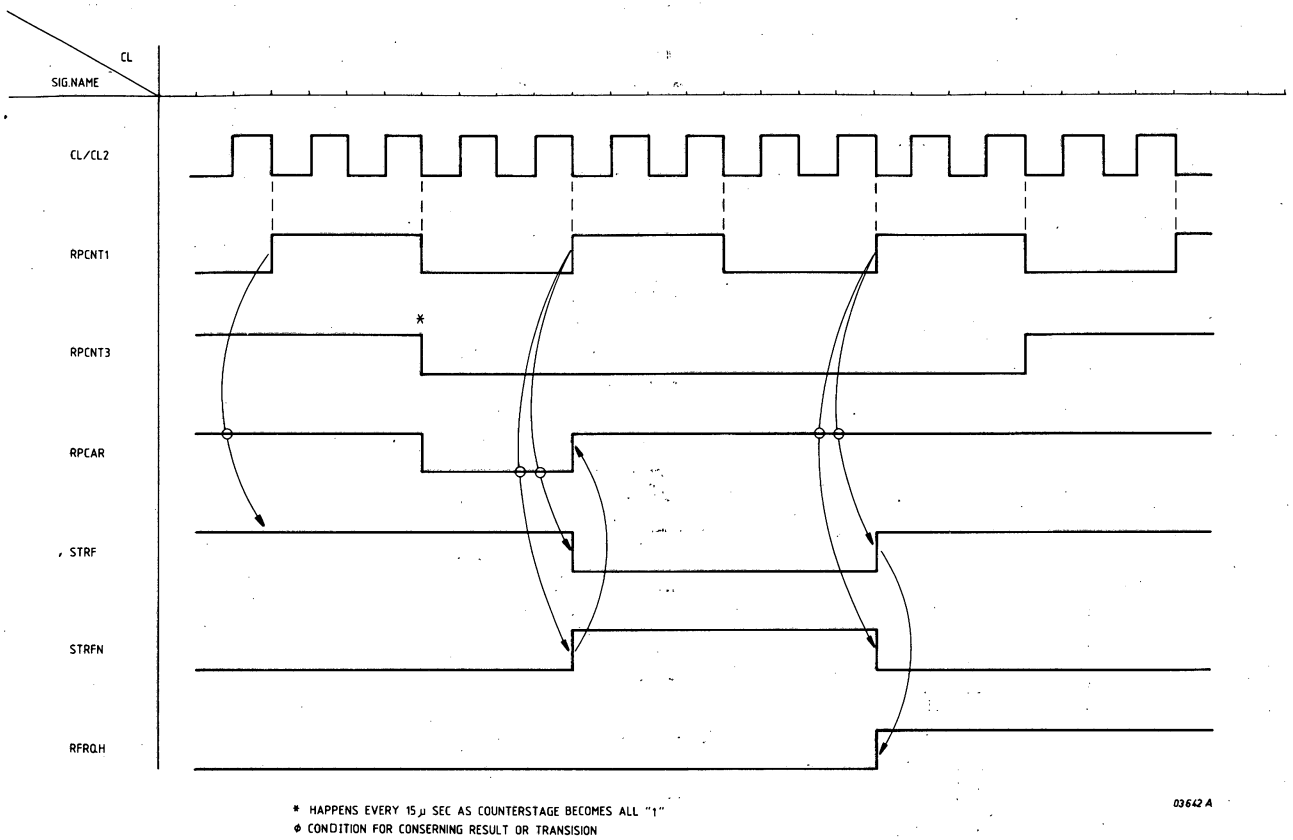


Figure 3.13 TIMING DIAGRAM OF SETTING HIDDEN REFRESH CONDITION

About the same happens as a hidden refresh is performed.
During the read or write cycle part I of equation (1) becomes "1" and EARFRON to "0". The same lock as for the automatic refresh occurs as part IV of eq. (1) becomes "1". As the concerning read or write cycle is finished a refresh cycle is performed with the only difference with the automatic refresh cycle, that now the hidden-FF will be reseted b.m.o. RRFRQHN. In the automatic refresh cycle reset was prevented by ERFRQN.
As in the automatic refresh cycle RFE becomes active by signal RFRQN to "0" now it has to wait till the read or write cycle is finished (RAS to "0").
Figure 3.15 gives the timing diagram of a hidden refresh cycle.

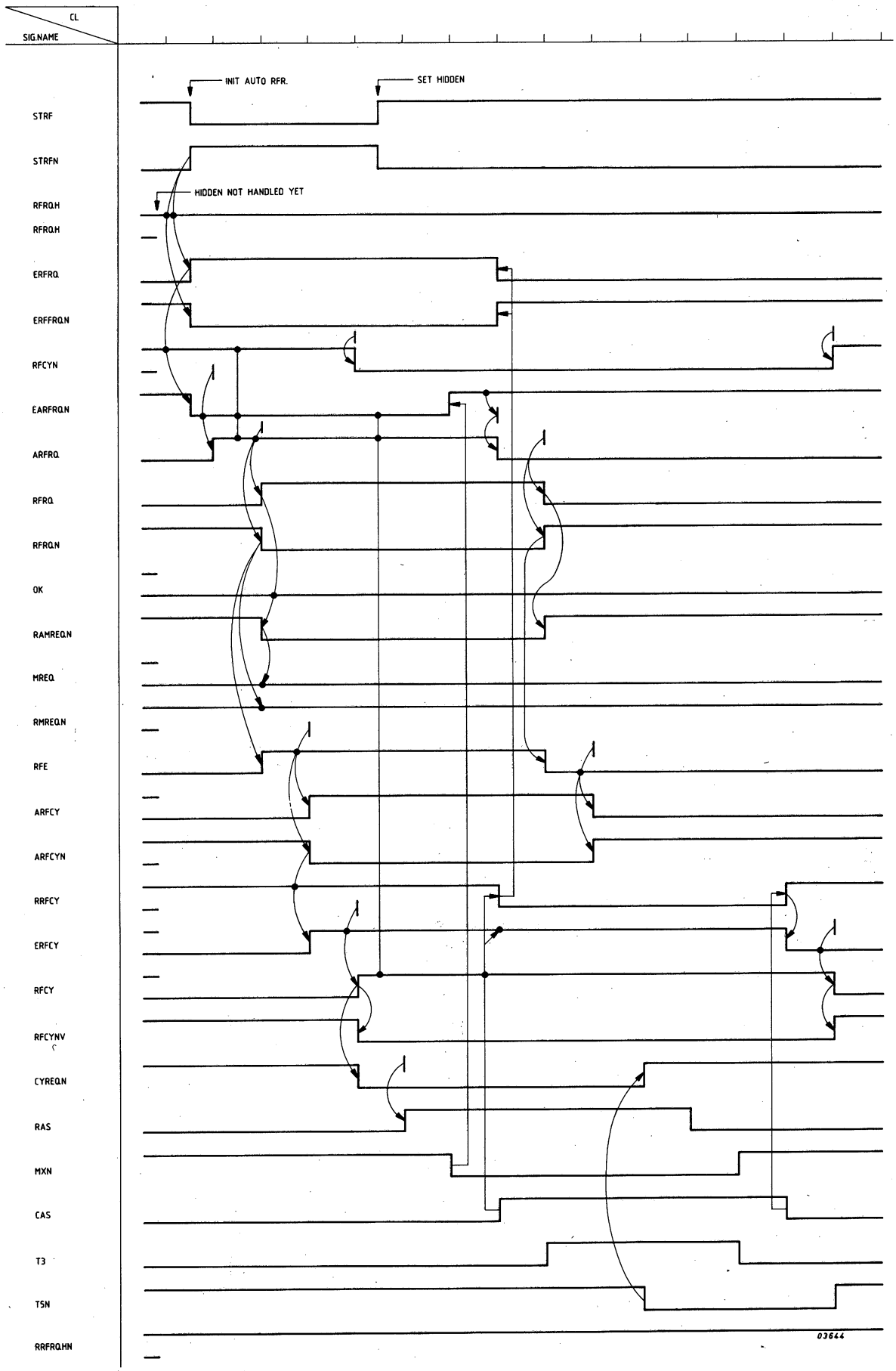


Figure 3.14 TIMING DIAGRAM AUTOMATIC REFRESH CYCLE

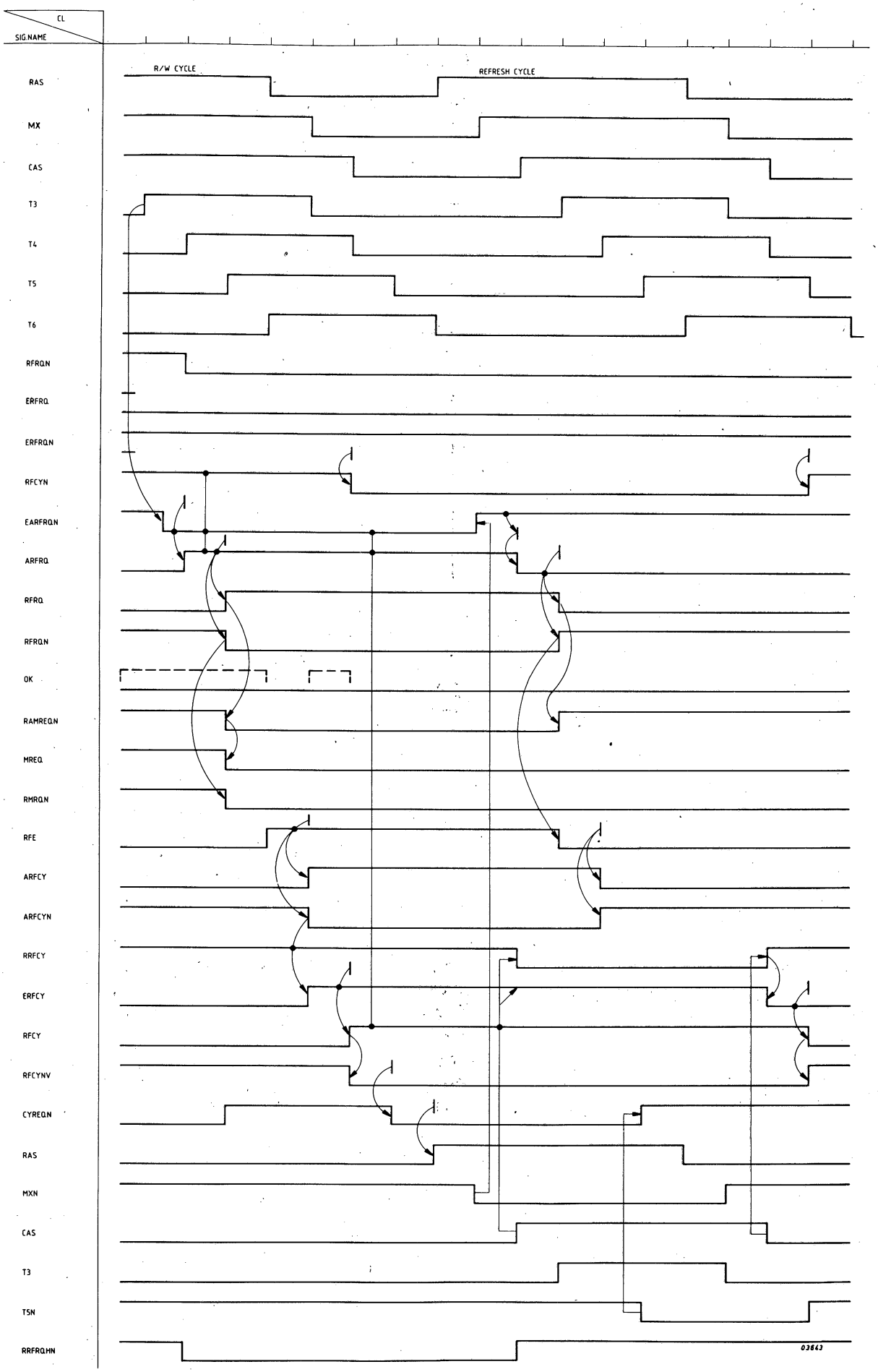


Figure 3.15 TIMING DIAGRAM HIDDEN REFRESH CYCLE

3.4.5 BUS TIMING

Main signals for bus timing are TMRN as a module R/W request signal and TSMN /ACN as a response of this request.
Below circuit diagram for generating TSMN and ACN is given.

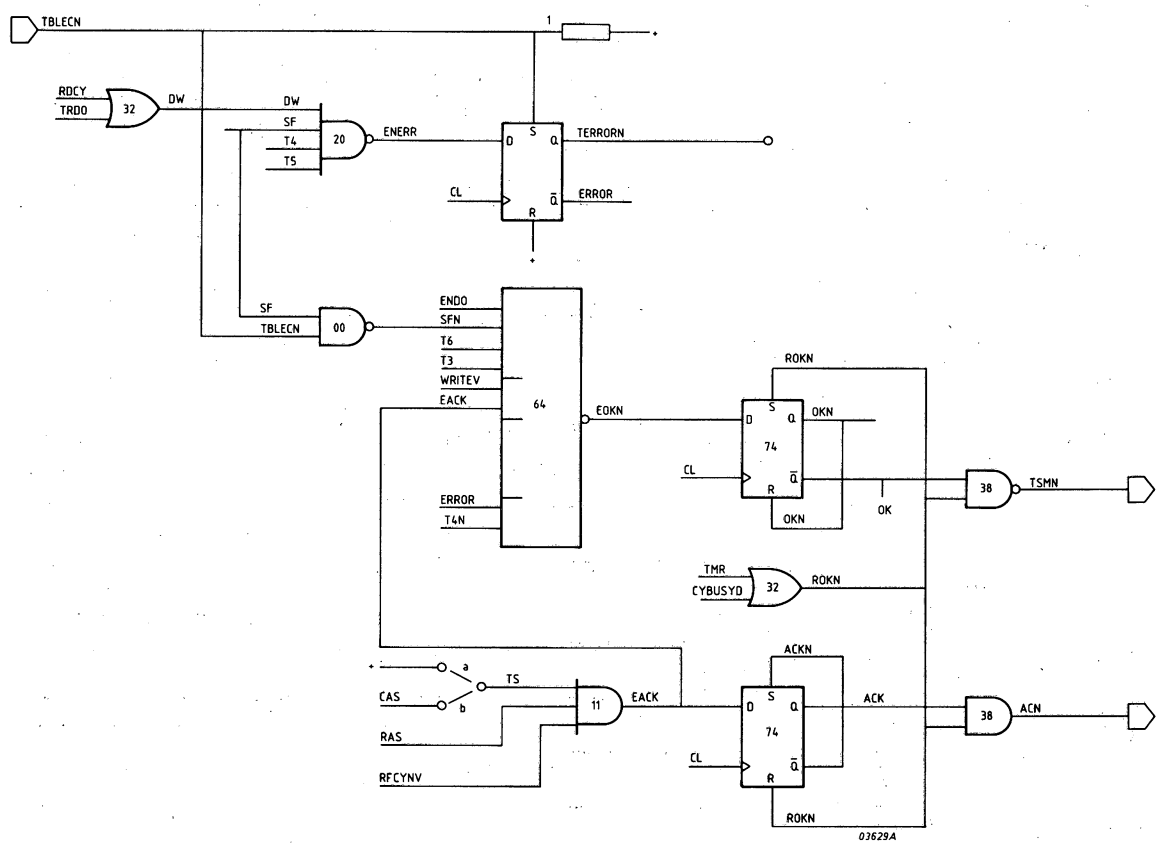


Figure 3.16 BUS TIMING CONTROL LOGIC

ACN

The requirement for the ACN accesstime is greater than or equal to 130ns.
To have a maximal result t_{ACN} is choosen as small as possible; this includes an adjustment due to speed versions of the module. Adjustments are indicated in figure 3.16 with a and b. For the normal speed version interconnection a. is present and for the high speed versions connection b. Condition RFCYNV on the 74S11 prevents that EACK is given during a refresh cycle. About one clock period after EACK became active ACK and ACN are true. ACKN locks the acknowledge FF which is reset agian by ROKN.

TSMN

About one clock period EOKN became active TSMN is given (see figure 3.16).

$$\overline{EOKN} = \underbrace{ENDO.SFN.T3.T6}_{I} + \underbrace{WRITEV.EACK}_{II} + \underbrace{ERROR.T4N}_{III}$$

Part I is only active during a read cycle; ENDO indicates that the request was intended for this module, it is a read cycle and no refresh is active.
SFN indicate if there is an error or not; if so (SFN=0), EOKN is not determined by part I as the cycle is now stretched and determined by part III.
Part II is active during a write cycle, timing is now the same as for ACN as EOKN is now determined by EACK.

3.4.6 CHARACTER CONTROL

As the module not only can operate in the word-mode (16 bits) but also in the character mode (8 bits) signals MAD15 and CHA are present to control this.

Mode		CHA	MAD15
Word	-	0	X
Character	LC	1	0
	RC	1	1

At the start of a module request this word/character data is clocked into a LS175 circuit as indicated below. B.m.o. S00/S32 circuits the signals ERCH, ERCHN and ELCH are derived.

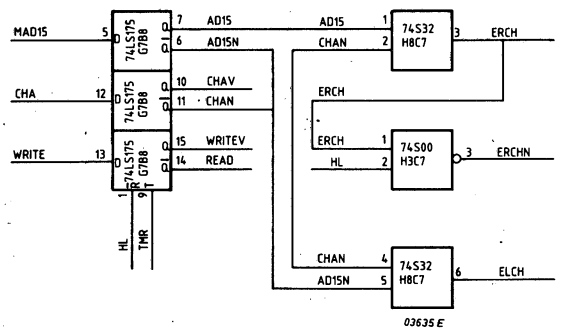


Figure 3.17 CHARACTER CONTROL LOGIC

3.4.6.1 DATA OUT

As already mentioned before, data transmission during a read character is always done by the right character. Figure 3.18 gives how the transmit data out signals TRDOR and TRDOL are generated.

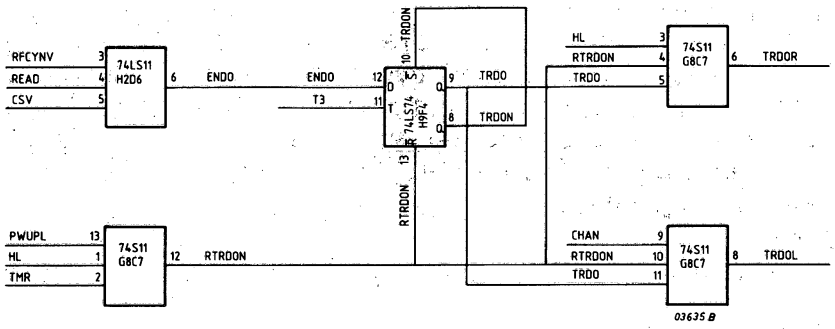


Figure 3.18 CHARACTER CONTROL LOGIC

CHAN ensures that in character mode TRDOL=0 with the result that the left character driver (to BIO 00:07N) is in the high impedance state.
Data is set on the bus as T3. The output driver FF is reset again as the module R/W request (TMR) is finished.

3.4.6.2 DOUBLE CYCLE

A special item in the character mode is the double cycle during a write character, as before the write action a read has to take place as the error correction is over both characters. During a write character signal RDCY becomes "1" (see figure 3.19) which indicates a double cycle.

WCY which is normal high during a write cycle is now held low so a read cycle is performed. The condition RDCY on the arbiter (see figure 3.19) ensures that after this read cycle the write cycle is performed. RDCY is set in this cycle to zero again by CYBUSYC.

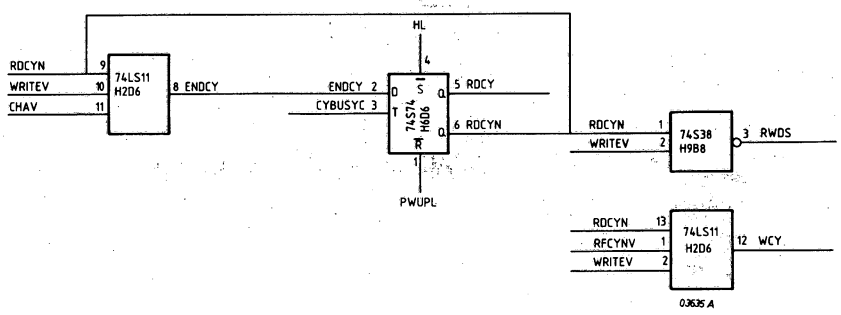


Figure 3.19 CHARACTER CONTROL LOGIC

3.4.7 MEMORY CYCLE MODES

In this part the timing diagrams are given for the modes and combinations which the module can perform.
Figure 3.20 gives the timing diagram for a write word without interference of refresh.
Figure 3.21 gives the timing diagram for a read word or character without errors.
Timing diagram for a write character is given in figure 3.24 here a double cycle is performed (read before write) as the error correction is done for 16 bits.
In part 3.4.4.4 detailed timing diagrams for hidden and automatic refresh cycle are given. To give a clear view what happens during a read cycle in case of an error figure 3.22 gives the part of interest for a cycle without an error (see also figure 3.22) and in case of an error. In case of no-error EOKN is determined by T3 and T6 because SFN=1; SFN becomes "0" in case of an error so now EOKN is determined by ERROR and T4N. The result is a shift of 2 clocks of TSMN in case of an error.
This delay of two clocks is sufficient to correct the data before TSMN becomes low.

3.4.8 CYCLE MODE COMBINATIONS

In this part combinations between R/W-requests and refresh requests are described as for as necessary.

1) R/W cycle -Hidden Refresh -R/W cycle.
   This combination is for a great part given in part 3.4.4.4 and figure 3.15. The result of this combination is that the last R/W cycle is delayed for maximum one cycle: during the first R/W cycle where the refresh is initiated, following R/W requests are blocked till the refresh cycle is finished.

2) Automatic Refresh-R/W cycle-Hidden Refresh.
   This combination occurs as during the automatic refresh cycle as R/W reuest enters. As the hidden FF is still set a hidden refresh is initiated during the R/W cycle. Figure 3.23 indicates till which moment the R/W cycle is handled BEFORE the automatic (see also figure 3.14).
   As the memory request signal TMRN is too late to start a cycle start (RAS) the automatic refresh is handled before the R/W-cycle. The latest may have a delay of maximum one cycle.

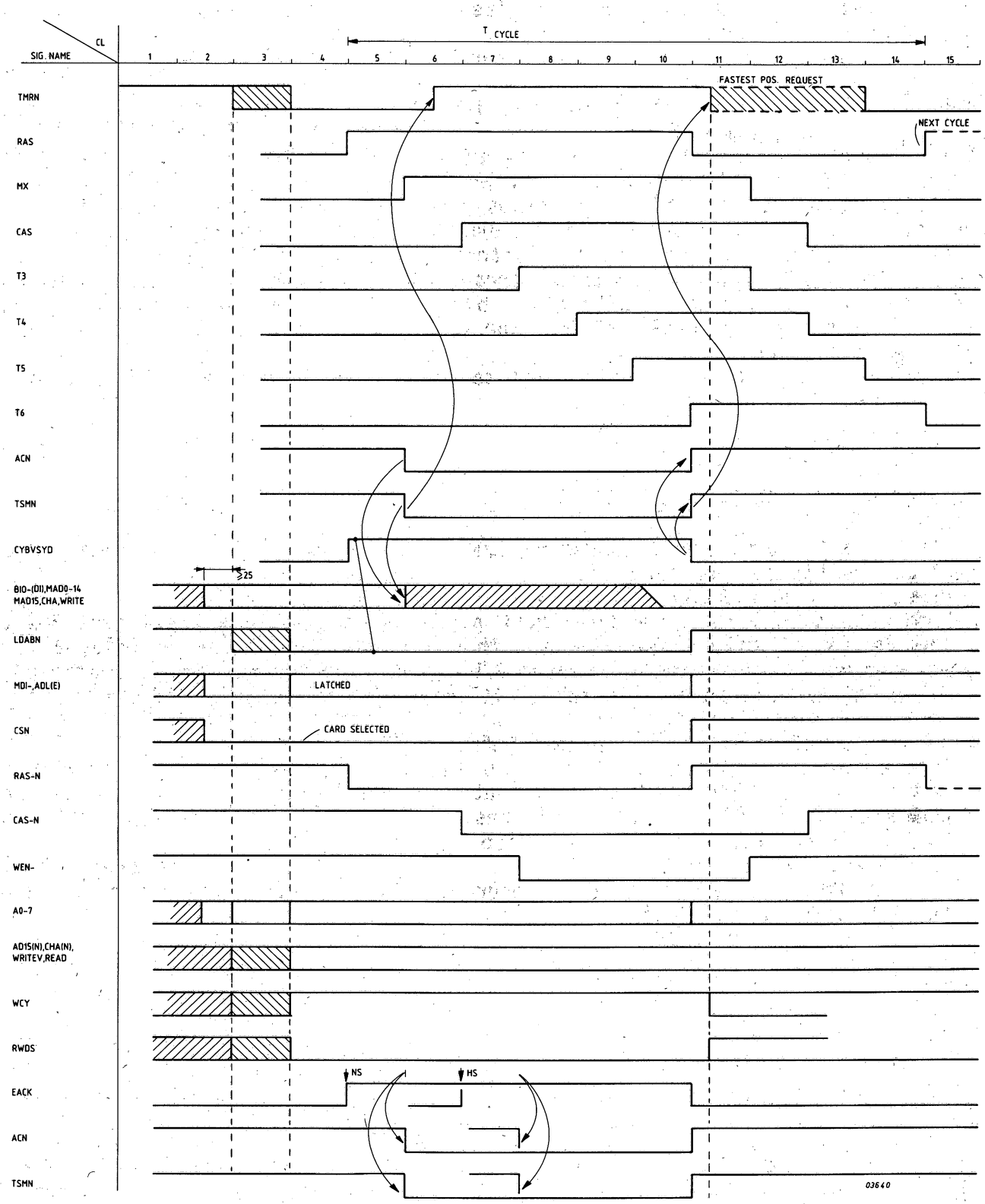


Figure 3.20 TIMING DIAGRAM WRITE WORD

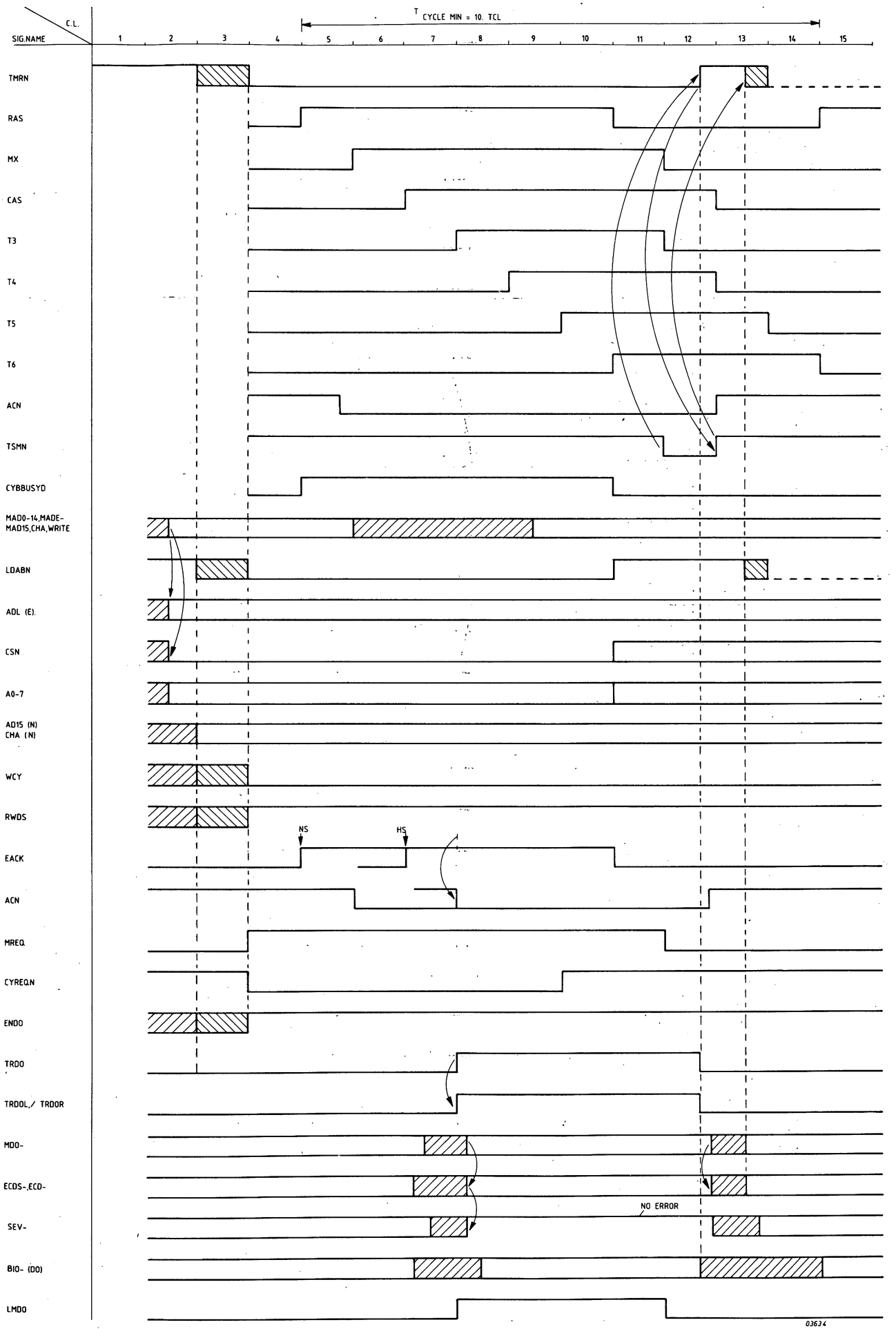


Figure 3.21 TIMING DIAGRAM READ WORD/CHARACTER

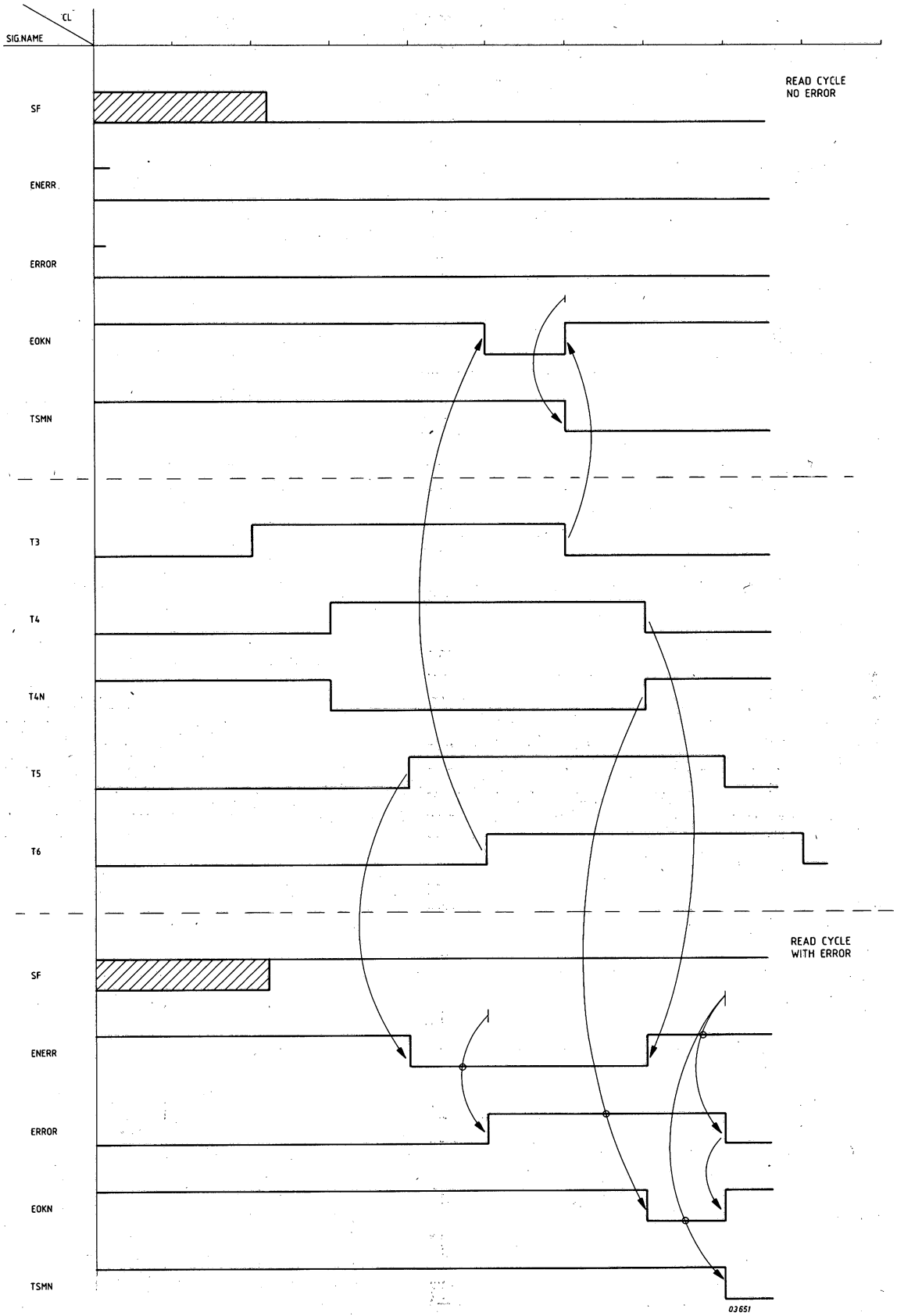


Figure 3.22 TIMING DIAGRAM READ CYCLE

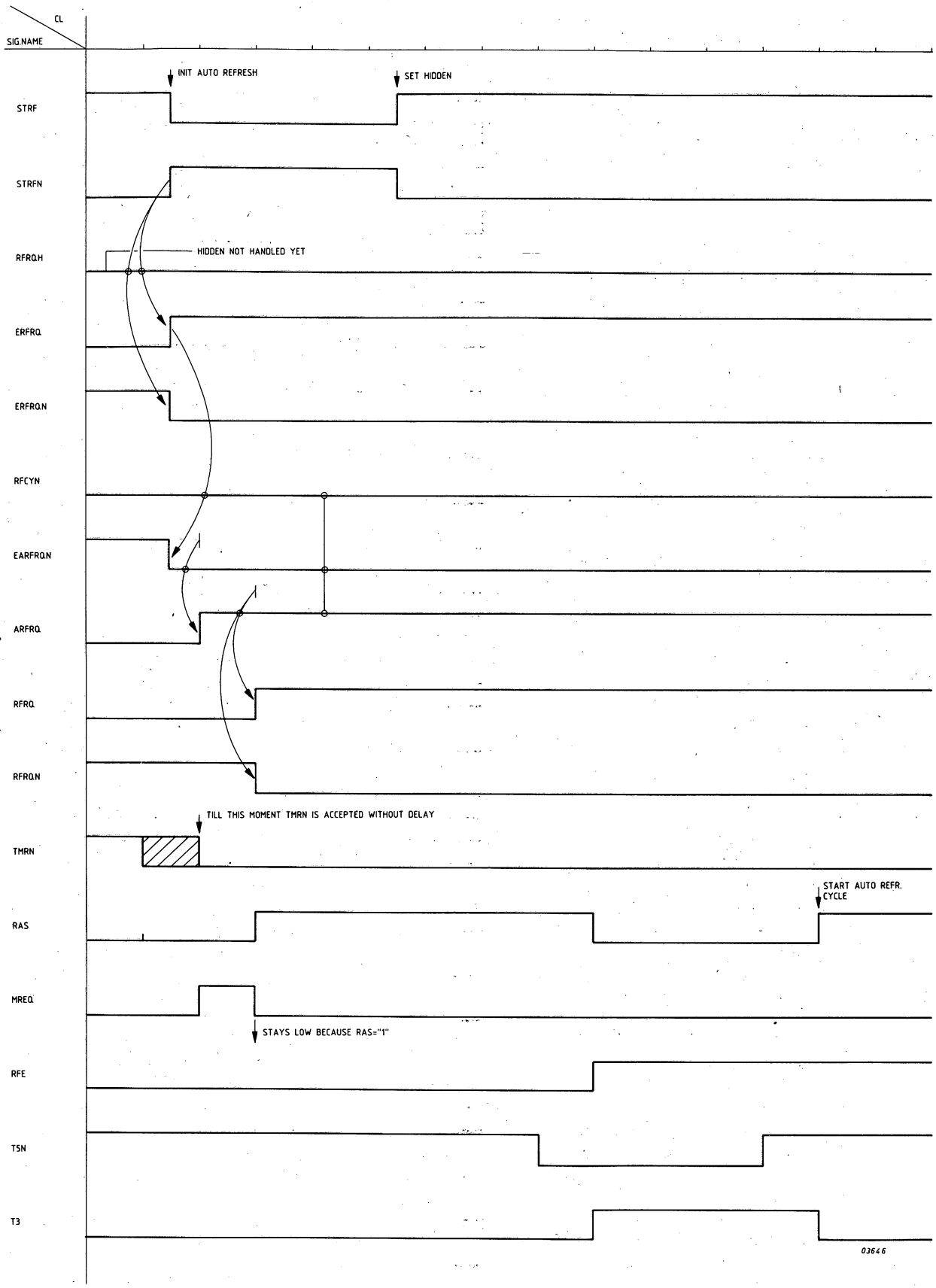


Figure 3.23 AUTOMATIC REFRESH AFTER DATA I/O

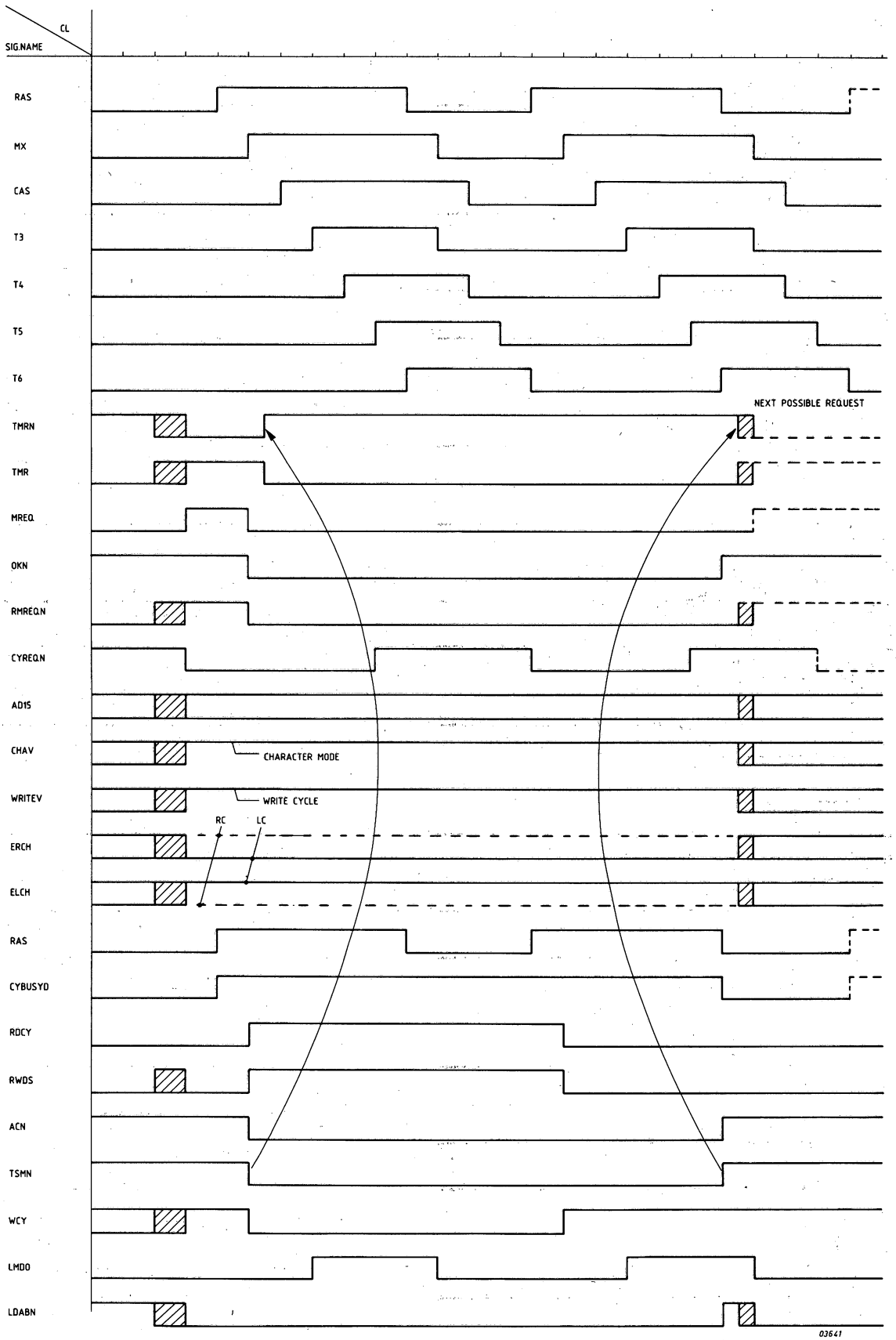


Figure 3.24 TIMING DIAGRAM WRITE CHARACTER

3.4.9 POWER SUPPLY AND BATTERY BACK-UP

As described elsewhere the memory is supplied with two +5 Volt supplies, one for the circuits which have to stay on in case of power break down, called B5PU (B is for Battery) and one for the other circuits called P5PU (P is for Power).
During normal system operation all supplies are valid and the RSLN (Reset Line Not) signal is high.
In the power/battery stand by mode, respectively due to machine switch off or power break down, the RSLN signal will become low to indicate power down. This forbids the start of any new cycle except Refresh cycle of course, and sets some control signals.
After RSLN low, the P5PU will be switched off, while the B5PU will be kept valid either by a separate power supply directly connected to the mains or by battery back-up.
All devices marked with a 'B' in a corner on figure 4.2 thru 4.5 are connected to the battery B5PU.
It can be seen now in the diagram that all the refresh and addressing logic is still working and that the data I/O circuitry and their related timing and control circuits are down.
By means of this stand by battery option, information of the memory is not lost in case of power down, while power consumption is reduced to a minimum.

DECOUPLING MEMORY ARRAY

Although the number of decoupling capacitors in the memory array is less than suggested by the device manufacturers for dynamic arrays on double sided prints, the high frequency interference is well within limits due to the multilayer board.

LIST OF ILLUSTRATIONS

FIGURE	4.1	BLOCK DIAGRAM WMD-1	PAGE 4-3
	4.2	ADDRESS GENERATION AND DECODING	4-5/6
	4.3	TIMING AND REFRESH	4-7/8
	4.4	ERROR CORRECTION	4-9/10
	4.5	DATA FLOW	4-11

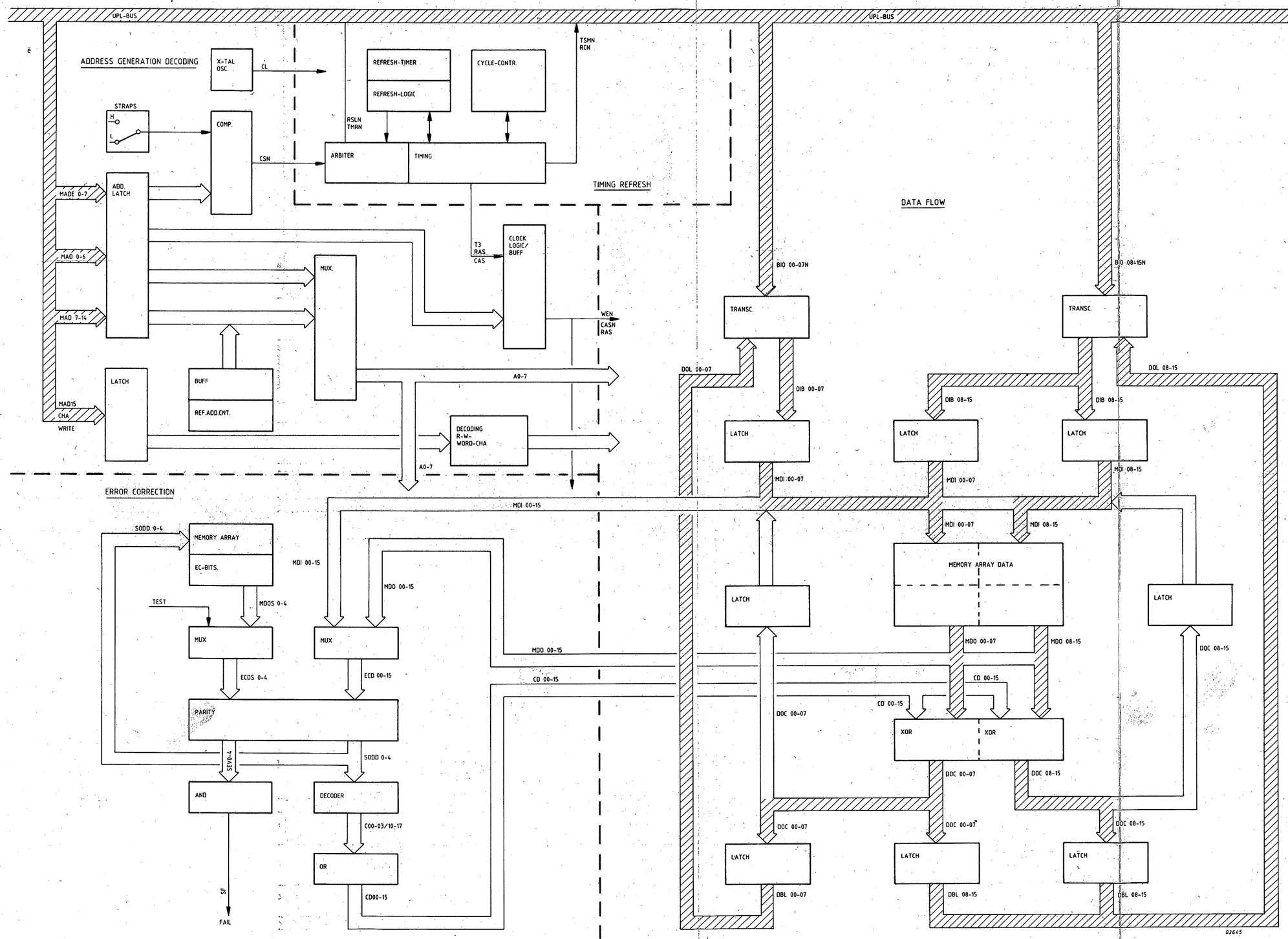
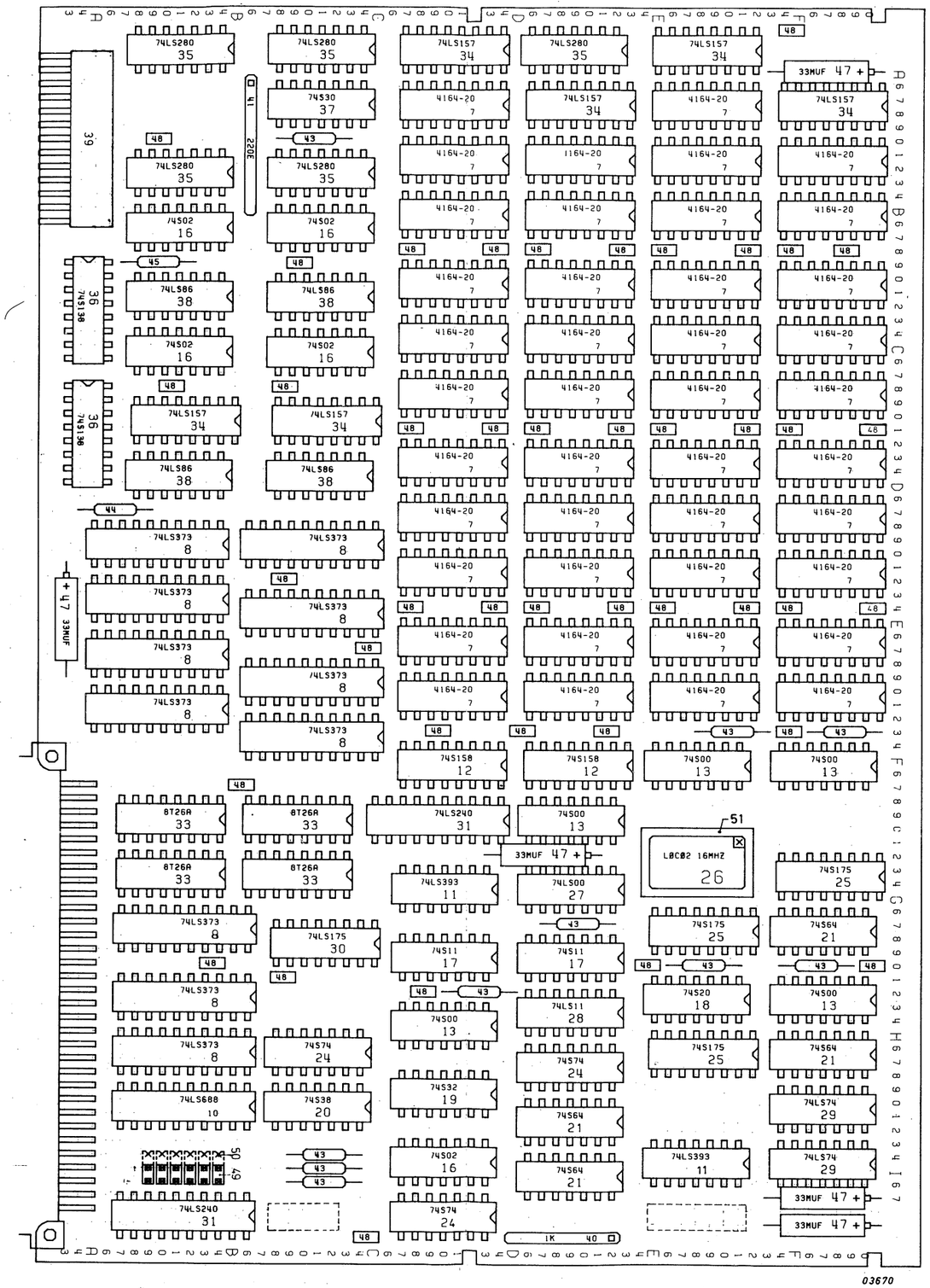


Figure 4.1 BLOCK DIAGRAM WMD-1


74LS280 35
74S30 37
74S02 16
74LS86 38
74LS157 34
74LS373 8
74LS158 12
74S00 13
74LS240 31
74LS393 11
74S11 17
74LS00 27
74LS11 28
74S74 24
74S32 19
74S64 21
74LS175 25
74S20 18
74LS74 29
74S38 20
74LS688 10
8T26A 33
74S158 12
74LS175 30
4164-20 7
L8C82 16MHZ 26
74S175 25
74S64 21
74S00 13
74S74 24
74S02 16
74LS240 31
74LS373 8
74LS74 29
74LS393 11
74S11 17
74S00 13
74S64 21

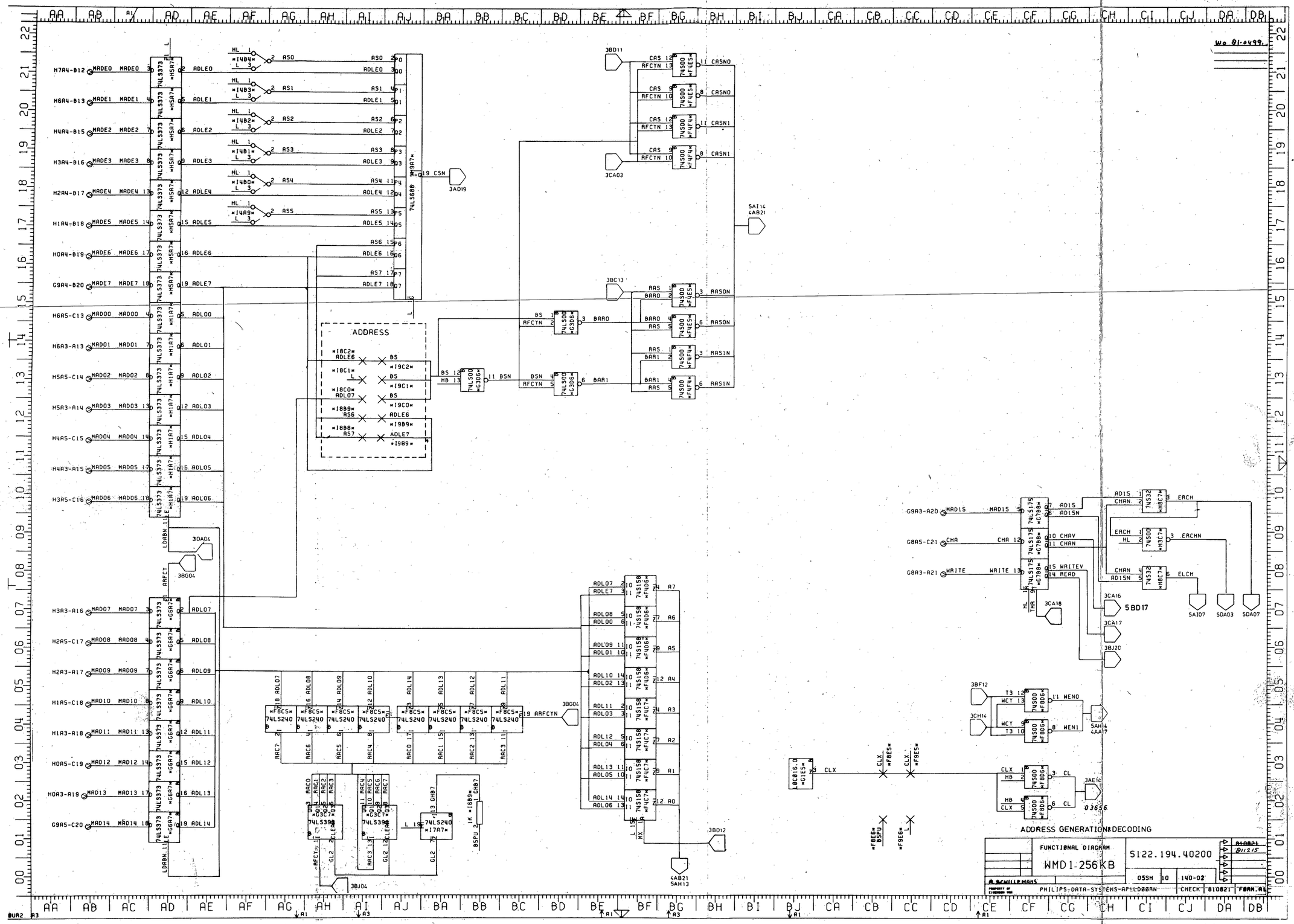


Figure 4.2 ADDRESS GENERATION AND DECODING

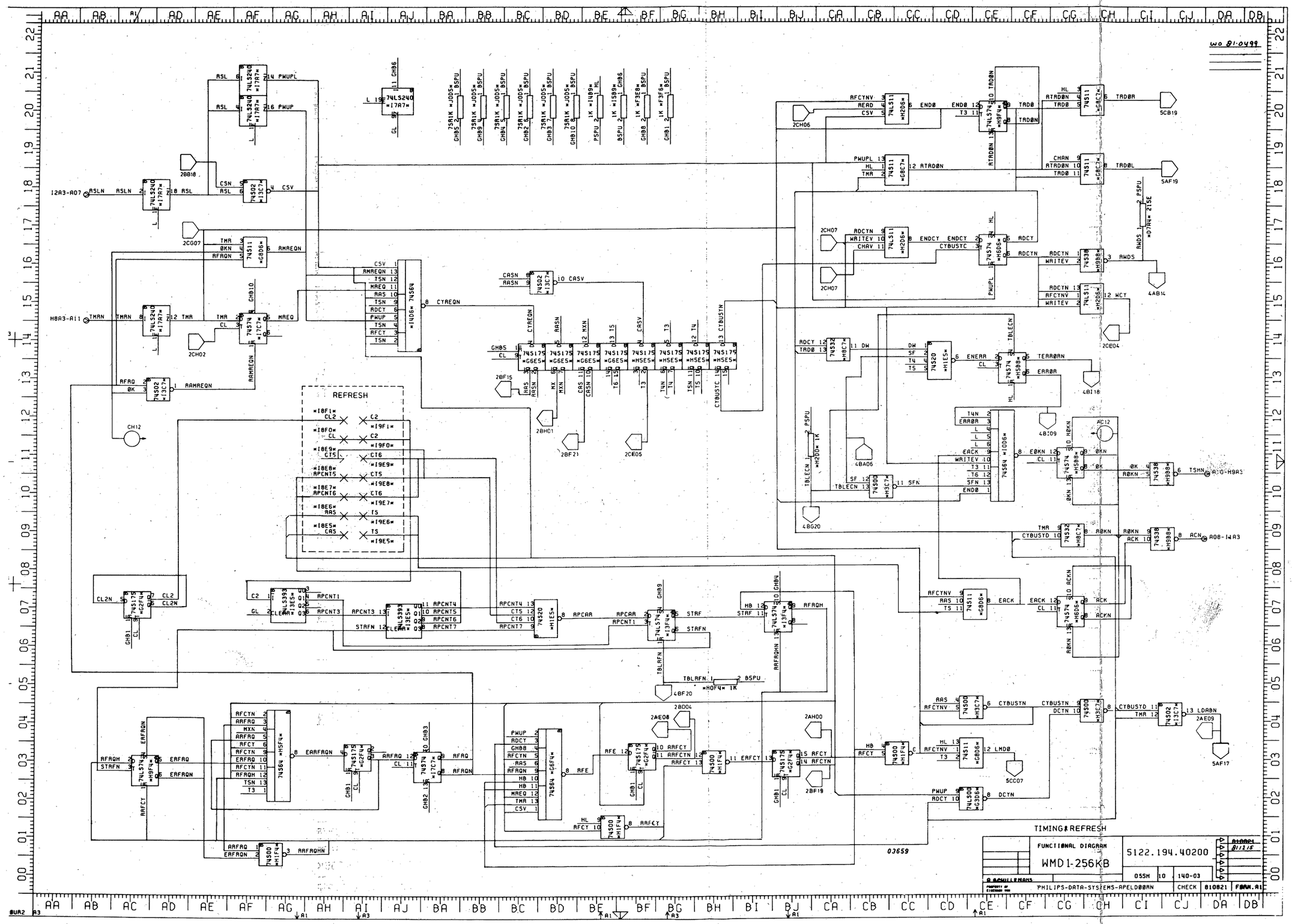


Figure 4.3 TIMING AND REFRESH

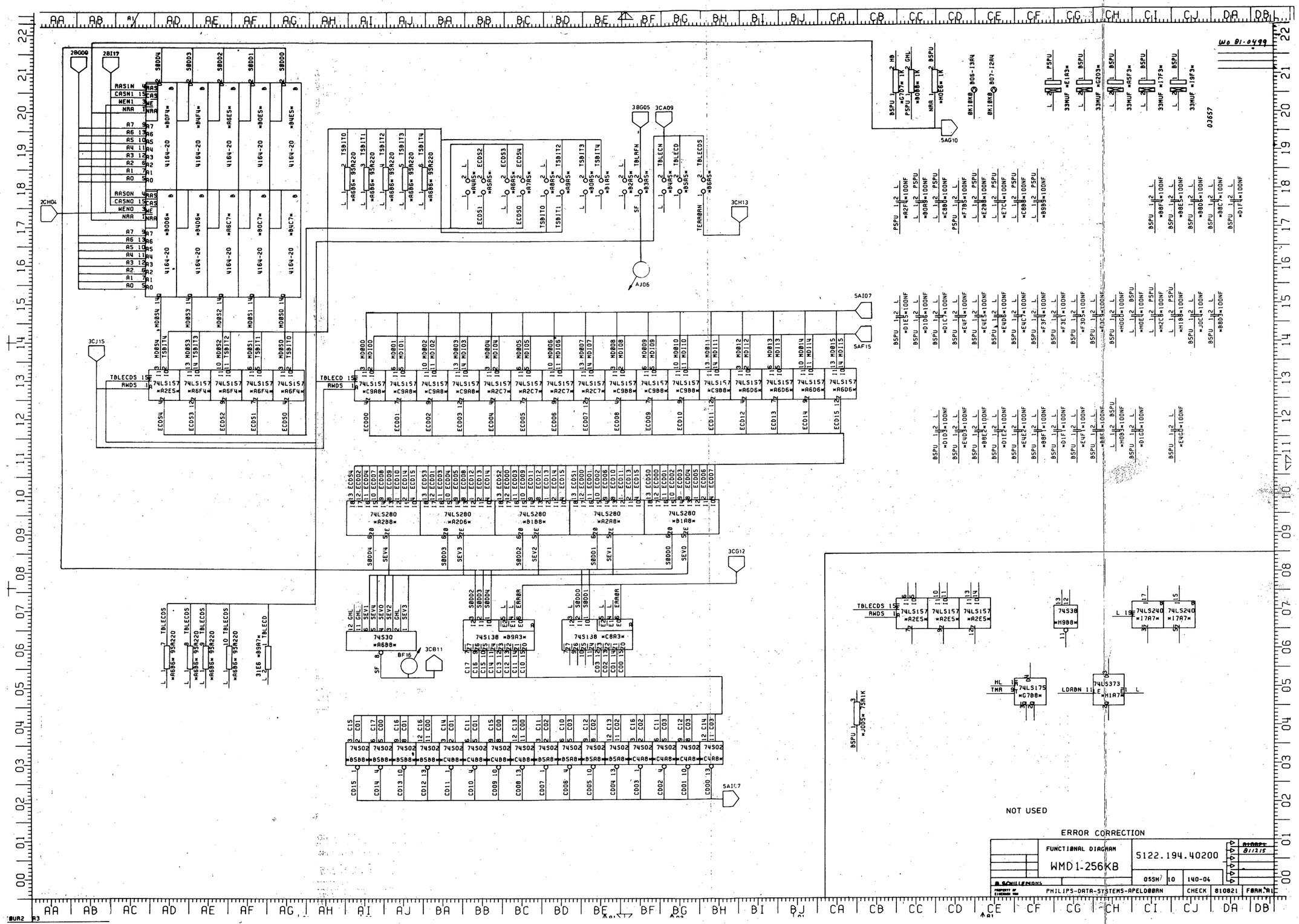


Figure 4.4 ERROR CORRECTION

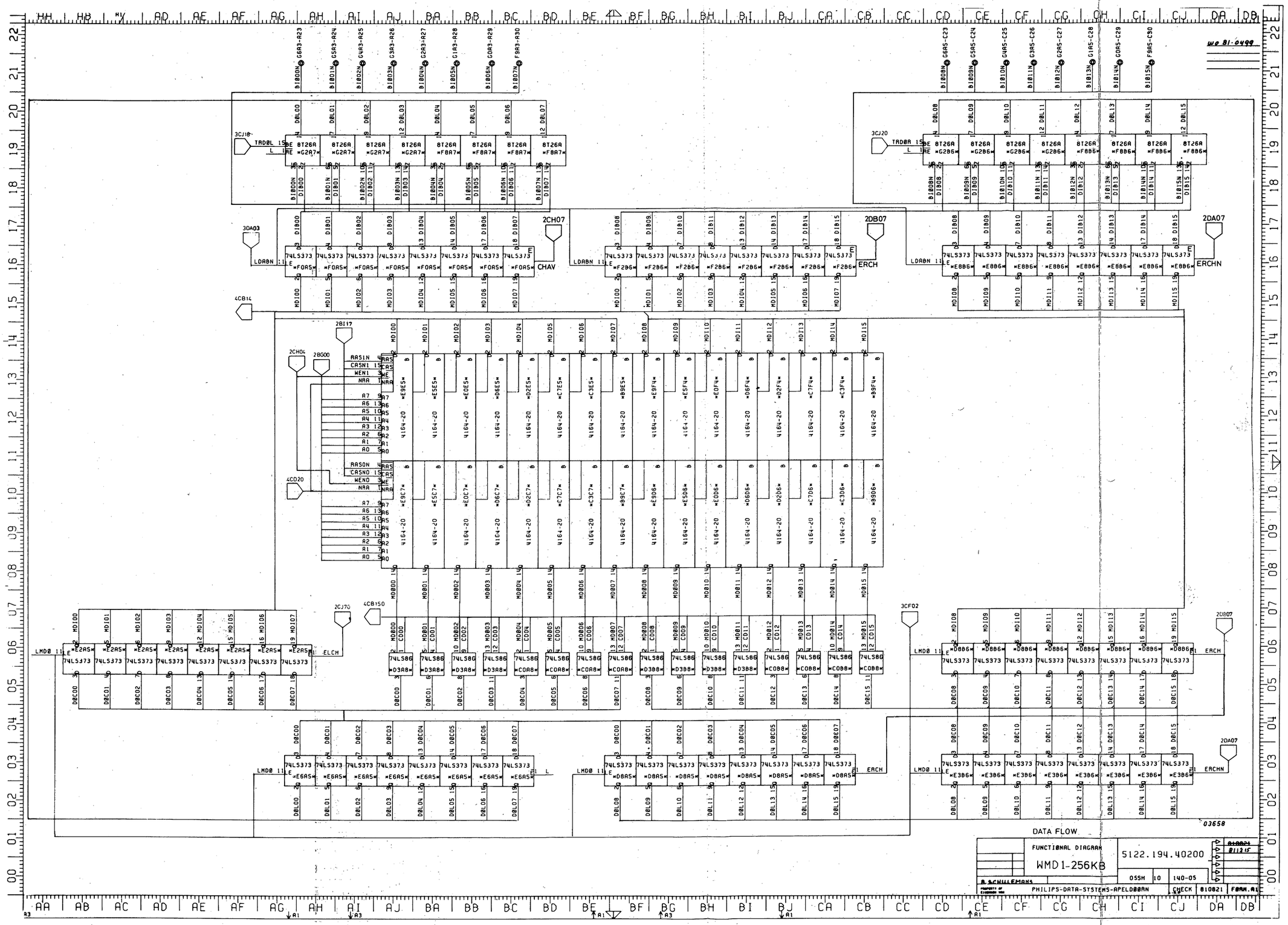
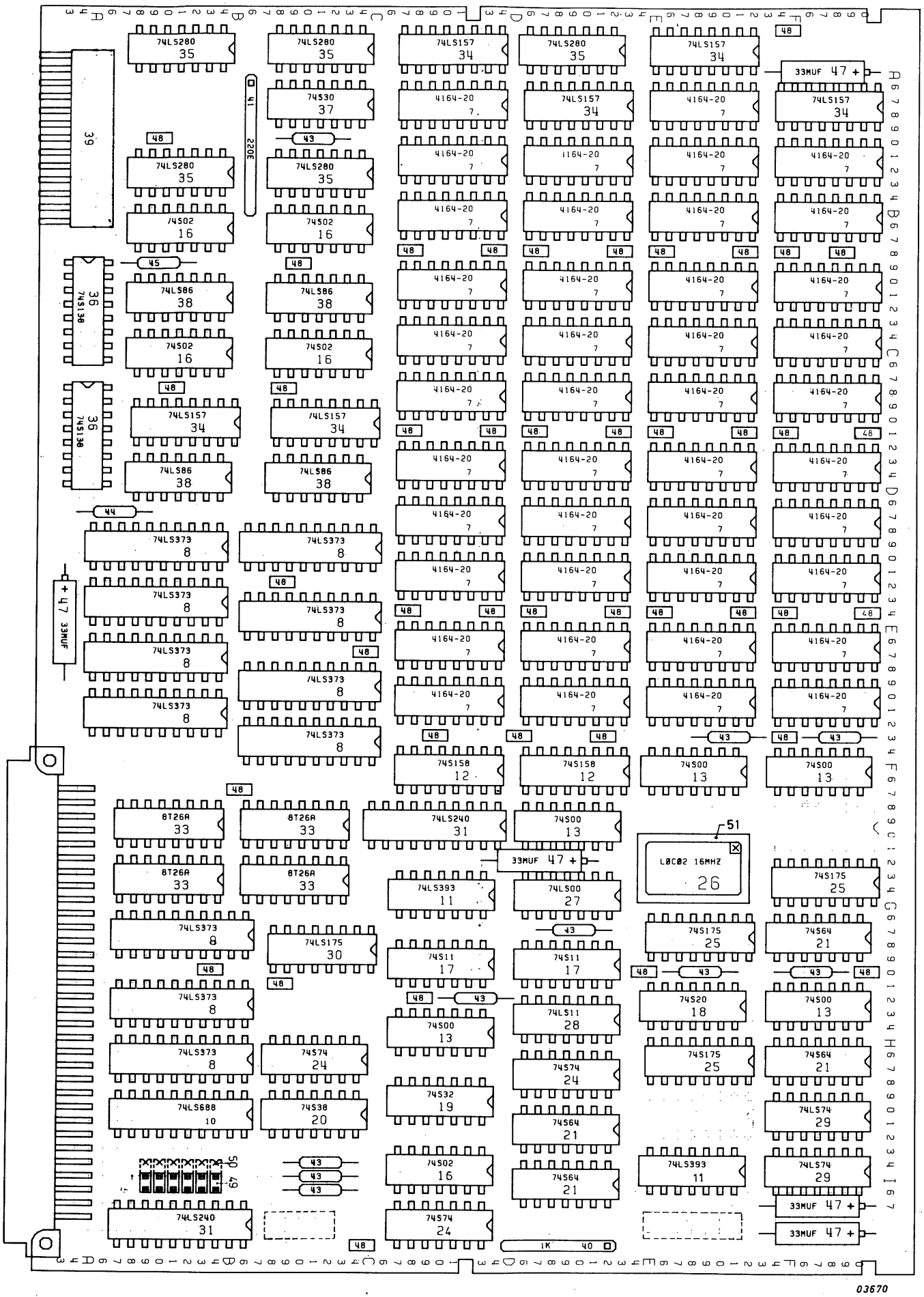


Figure 4.5 DATA FLOW

6 PARTS LIST


74LS280 35
74LS157 34
74S30 37
74S02 16
74LS86 38
74LS373 8
74S158 12
74S00 13
8T26A 33
74LS240 31
74LS393 11
74LS00 27
74LS175 30
74S11 17
74LS11 28
74S20 18
74S74 24
74S32 19
74S38 20
74LS688 10
74S64 21
74LS74 29
74LS393 11
74S175 25
74S64 21
74S00 13
74S74 24
74LS240 31
74S02 16
74S64 21
74LS393 11
74LS74 29
33MUF 47 +
LØCØ2 16MHZ 26
51
39
36 74S138
36 74S138
41 220E
+ 47 33MUF
1K 40
03670

Pos.	Code Number	Description
A	5122 194 40200	PCB WMD1 compl.
7B	5122 000 12930	IC 4164-20
8B	5122 000 10130	IC 74LS373
10B	5122 000 12750	IC 74LS688
11B	5122 000 10760	IC 74LS393
12B	5122 000 10050	IC 74S158
13B	5122 000 10080	IC 74S00
16B	5122 000 10780	IC 74S02
17B	5122 000 10090	IC 74S11
18B	5122 000 10100	IC 74S20
19B	5122 000 10820	IC 74S32
20B	5122 000 09960	IC 74S38
21B	5122 000 09650	IC 74S64
24B	5122 000 10110	IC 74S74
25B	5122 000 10900	IC 74S175
26B	5122 000 11320	LOCO 16MHz.
27B	5122 000 09120	IC 74LS00
28B	5122 000 09130	IC 74LS11
29B	5122 000 09150	IC 74LS74
30B	5122 000 09710	IC 74LS175
31B	5122 000 10600	IC 74LS240
33B	5122 000 09520	IC 8T26
34B	5122 000 09200	IC 74LS157
35B	5122 000 10680	IC 74LS280
36B	5122 000 09250	IC 74S138
37B	5122 000 10810	IC 74S30
38B	5122 000 10410	IC 74LS86
39B	5122 000 12870	Connector 26 pol. (MP75789)
40B	5122 000 11490	Resistor network 1K
41B	5122 000 11740	Resistor network 220E
43B	2322 151 51002	Resistor 1K
44B	2322 151 52151	Resistor 215E
45B	2322 151 53169	Resistor 31E6
47B	2022 001 00142	Elco 33uF - 10V
48B	5122 000 11820	Capacitor 100nF - 25V
49B	2411 024 13001	Female plug 2 pol.
50B	2411 011 07257	Male plug 3 pol.
51B	5122 110 91490	Oscillator socket

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2022 001 00142	5322 124 14053	ELCO C33MU/15V
2322 151 51002	4822 116 51235	RES.1K MR25
2322 151 52151	5322 116 55274	RES.215E +-1% 0,125W
2322 151 53169	5322 116 54034	RES. 31,6E 0,4W
5122 000 09120	5322 209 84823	IC N74LS00A
-		
5122 000 09130	5322 209 85604	IC N74LS11A
5122 000 09150	4822 209 80782	IC 74LS74
5122 000 09200	5322 209 85489	IC N74LS157B
5122 000 09250	5322 209 85672	IC N74S138B
5122 000 09520	5322 209 85608	IC N8T26AN
-		
5122 000 09650	5322 209 84724	IC SN74S64N
5122 000 09710	5322 209 84999	IC SN74LS175N-00
5122 000 09960	5322 209 85677	IC N74S38A
5122 000 10050	5322 209 85759	IC 74S158
5122 000 10080	5322 209 84167	IC SN74S00N-00
-		
5122 000 10090	5322 209 84915	IC N74S11N
5122 000 10100	5322 209 85195	IC SN74S20N
5122 000 10110	5322 209 84183	IC SN74S74N-00
5122 000 10130	5322 209 86062	IC SN74LS373J
5122 000 10410	5322 209 84997	IC SN74LS86N-00
-		
5122 000 10600	5322 209 85862	IC SN74LS240N
5122 000 10680	5322 209 85875	IC SN74LS280N
5122 000 10760	4822 209 80447	IC N74LS393N
5122 000 10780	5322 209 85407	IC N74S02A
5122 000 10810	5322 209 85194	IC SN74S30N
-		
5122 000 10820	5322 209 85679	IC N74S32A
5122 000 10900	5322 209 85451	IC N74S175B
5122 000 11320	5322 242 74379	OSILATOR 16MHZ
5122 000 11490	5322 111 94227	RES. 7SR 1K
5122 000 11740	5322 111 94235	RES.9SR220
-		
5122 000 11820	5322 122 34153	CAP.100NF 50V
5122 000 12750	5322 209 80976	74LS688
5122 000 12980	5322 209 81241	IC HN 4864-3
5122 194 40200	5322 216 21091	PCB WMD

END OF REPORT